2026년 1월 28일(수), 09:00-10:45
Room A(4층, 그랜드볼룸 I+II)

D. Thin Film Process Technology 분과

O01_[WA1-D] High-k/Metal Gate

좌장: 이홍섭 교수(경희대학교), 백인환 교수(인하대학교)

초청발표 **WA1-D-1** 09:00-09:30	**How to Modulate Threshold Voltage (V_{th}) Using ALD HKMG Gate Stack for Advanced Logic Transistor and DRAM Peripheral Transistor** Changhwan Choi[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University
WA1-D-2 09:30-09:45	**A Study on a PECVD-Deposited SiCN Capping Layer in High-k/Metal-Gate** Hye-Ri Hong[1], Woon-San Ko[1], So-Yeong Park[1], Seong-Jo Jo[1], Myeong-Ho Song[2], and Ga-Won Lee[1] [1]Chungnam National University, [2]NNFC
WA1-D-3 09:45-10:00	**Leakage Current Reduction in HKMG Stacks through Nitridation Engineering** Chinsung Park, Hyungchul Kim, Seungwook Kim, Seungmi Lee, Yeongseok Jeong, Yunhyuck Ji, and Seungwoo Jin R&D Process, R&D Division, SK hynix Inc.
WA1-D-4 10:00-10:15	**Experimental Investigation of Al-Based Doping for Threshold Voltage Control of GAA pMOS Device** Wonjae Choi[1], Sangkuk Han[2], Haesoo Jang[1], Jaewon Chung[1], Sangmyun Lim[1], Kyungwook Park[2,3], Sangwoo Jeong[2], Soyoung Park[1], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University, [3]DRAM Process Development Team, Samsung Electronics Co., Ltd.
WA1-D-5 10:15-10:30	**Tuning the Effective Work Function of TiAlN Gate Electrodes through ALD Aluminum Incorporation** Hae-Dam Kim, Gyeong-Min Jeong, and Jin-Seong Park Division of Materials Science and Engineering, Hanyang University
WA1-D-6 10:30-10:45	**HfO_2, ZrO_2, and La_2O_3 Films Deposited by Liquid-Injection ALD for High-K Gate Dielectric Applications** Ji-Won Jang[1], Soon-Kyeong Park[1], Ye-Won Han[3], Hee-Sung Kang[4], and Il-Kwon Oh[1,2] [1]Department of Intelligence Semiconductor Engineering, Ajou University, [2]Department of Electrical and Computer Engineering, Ajou University, [3]Department of Materials Science & Chemical Engineering, Hanyang University ERICA, [4]RPM Team, R&D Innovation Center, MKP Inc.

2026년 1월 28일(수), 09:00-10:45
Room B(4층, 그랜드볼룸 III)

K. Memory (Design & Process Technology) 분과

O02_[WB1-K] NAND Flash

좌장: 심원보 교수(서울과학기술대학교), 김윤 교수(서울시립대학교)

초청발표 **WB1-K-1** 09:00-09:30	**Reliability Issues and Modeling of 3D NAND Flash Memory** Sangmoo Choi, Kyoungjin Park, Kyoungcheol Kwon, Hyun Heo, Juyeab Lee, and Jumsoo Kim SK hynix Inc.
WB1-K-2 09:30-09:45	**밴드갭 엔지니어링 산질화 붕소(Boron Oxynitride, BON) 터널링 층을 이용한 고성능 및 고신뢰성 3D NAND Flash Memory** 강대현[1], 정재중[1], 박영근[1], 김영준[2], 조병진[1,2] [1]한국과학기술원 전기 및 전자공학부, [2]한국과학기술원 반도체공학대학원
WB1-K-3 09:45-10:00	**A Novel Approach to Enhancing Cell Current in 3D NAND Using Backside Channel Engineering** Yeeun Kim[1], Jaejoong Jeong[2], Byung Jin Cho[2], and Jong Kyung Park[1] [1]Department of Semiconductor Engineering, Seoul National University of Science & Technology, [2]School of Electrical Engineering, KAIST
WB1-K-4 10:00-10:15	**저유전율 마카로니 필러 적용을 통한 3D NAND Flash Memory 의 GIDL Erase 특성 향상** 김민승[1], 정재중[1], 김승훈[1], 강대현[1], 유찬미[2], 조병진[1,2] [1]한국과학기술원 전기 및 전자공학부, [2]한국과학기술원 반도체공학대학원
WB1-K-5 10:15-10:30	**Impact of Crystallization on Trap Levels and Charge Storage Characteristics of High-k HfO_2 Charge Trap Layers for 3D NAND Flash Memory Device** Dohyun Lee[1], Yunseo Lim[2], Jisu Park[1], Gyumin Hwang[1], Sangmyun Lim[1], Seongho Lee[2], JinYeong Lee[1], Hoon Pyo[1], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University
WB1-K-6 10:30-10:45	**실리콘 질화물 내 저마늄 도입을 통한 CTF 소자의 메모리 특성 개선** 신건희[1], 박영근[2], 정재중[2], 김희태[2], 김승훈[2], 강대현[2], 박동욱[2], 정원묵[2], 김민승[2], 유찬미[1], 이동규[1], 조병진[1,2] [1]한국과학기술원 반도체공학대학원, [2]한국과학기술원 전기 및 전자공학부

2026년 1월 28일(수), 09:00-10:45
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O03_[WC1-D] Memory Capacitors I

좌장: 이웅규 교수(숭실대학교), 문태환 교수(아주대학교)

초청발표 **WC1-D-1** 09:00-09:30	**How Can We Stabilize Metastable Rutile TiO_2 Films on Any Substrate?** Seong Keun Kim[1,2] [1]Electronic and Hybrid Materials Research Center, KIST, [2]KU-KIST Graduate School of Converging Science and Technology, Korea University
WC1-D-2 09:30-09:45	**Suppression of Low-k Interfacial Layer in ZrO_2/TiN Capacitors by Atomic Layer Deposition Using Ligand-Modified Zr Precursor** Hyeongjun Kim, Seungmin Jo, and Woongkyu Lee Department of Materials Science and Engineering, Soongsil University
WC1-D-3 09:45-10:00	**Sc Doping to Improve the Electrical Properties of TiO_2 Dielectric Thin Films** Seungwoo Lee[1], Soomin Yoo[1], Gaeul Kim[1], Hansol Oh[2], Hanbyul Kim[2], Donghun Shin[2], Yongjoo Park[2], and Woojin Jeon[1] [1]Department of Materials Science and Engineering, Kyung Hee University, [2]Advanced Research Development Team, SK Trichem Co., Ltd.
WC1-D-4 10:00-10:15	**Plasma-Enhanced Atomic Layer Deposition of Stable MoO_2 Thin Films for High-Performance TiO_2-Based DRAM Capacitors** Jae Hyeon Lee, Seon Gu Choi, Jeong Min Han, and Jeong Hwan Han Department of Materials Science and Engineering, Seoul National University of Science & Technology
WC1-D-5 10:15-10:30	**Upper-Layer-Induced Crystallization of Metastable Rutile TiO_2** Jihoon Jeon[1,2], Jongseo Kim[1,2], Seungwan Ye[1,2], and Seong Keun Kim[1,2] [1]Electronic and Hybrid Materials Research Center, KIST, [2]KU-KIST Graduate School of Converging Science and Technology, Korea University
WC1-D-6 10:30-10:45	**Strategy for Bottom-Electrode-Independent Stabilization of Rutile TiO_2 via ALD** Seungwan Ye[1,2], Jihoon Jeon[1,2], Jongseo Kim[1,2], Minseok Kim[1,2], and Seong Keun Kim[1,2] [1]Electronic and Hybrid Materials Research Center, KIST, [2]KU-KIST Graduate School of Converging Science and Technology, Korea University

2026년 1월 28일(수), 09:00-10:45
Room D(5층, 컨벤션홀 L)

J. Nano-Science & Technology 분과

O04_[WD1-J] 2차원 나노소재의 성장 및 물성 제어

좌장: 왕건욱 교수(고려대학교), 김준석 교수(홍익대학교)

초청발표 **WD1-J-1** 09:00-09:30	**Solution-Processed 2D Materials for Next-Generation Electronics** Joohoon Kang Department of Chemical and Biomolecular Engineering, Yonsei University
WD1-J-2 09:30-09:45	**Wafer-Scale Single-Crystal Growth of Bernal-Stacked Boron Nitride** Jaewon Wang[1], Hyeonwoo Lee[1], Jaemin Kim[2], Haeng Un Yeo[1], Cheol Hwan Yoon[1], Min Seok Yoo[3], Junseop Noh[1], Sora Jang[1], Ju-Hyoung Han[1], Juwon Han[1], Jaeeun Park[1], Young Ho Jin[1], Huijun Han[1], Kitae Park[1], Joonki Suh[4], Tae-Sik Yoon[1], Seunguk Song[5], Minsu Seol[3], Chanyong Hwang[6], Hyung-Joon Shin[1], Zonghoon Lee[1], Changwook Jeong[1], and Soon-Yong Kwon[1] [1]Department of Materials Science and Engineering and Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [2]Center for Multidimensional Carbon Materials, IBS, [3]2D Device Laboratory, Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd., [4]Department of Chemical and Biomolecular Engineering, KAIST, [5]Department of Energy Science, Sungkyunkwan University, [6]Quantum Technology Institute, KRISS
WD1-J-3 09:45-10:00	**Probing Nanoscale Structural Perturbation in WS_2 Monolayer via Explainable Artificial Intelligence** Hyeong Chan Suh[1], Jaekak Yoo[1], Kangmo Yeo[2], Dong Hyeon Kim[1], Yo Seob Won[3], Taehoon Kim[1], Youngwoo Cho[4], Ki Kang Kim[3], Seung Mi Lee[5], Heejun Yang[6], Dong-Wook Kim[7], and Mun Seok Jeong[1] [1]Department of Physics, Hanyang University, [2]Samsung SDI, [3]Department of Energy Science, Sungkyunkwan University, [4]Kim Jaechul Graduate School of Artificial Intelligence, KAIST, [5]KRISS, [6]Department of Physics, KAIST, [7]Department of Physics, Ewha Womans University
WD1-J-4 10:00-10:15	**High-Pressure CVD Growth of 2D Semiconductor with Minimized Defect Density** Takmo Jeong and Seok Joon Yun Department of Semiconductor Physics and Engineering, University of Ulsan
WD1-J-5 10:15-10:30	**Effect of Seed-Layer Morphology on Dielectric Interface and Device Performance in MoS_2 Field-Effect Transistors** Sumin Hong[1], Haksoon Jung[2], Sanghyun Lee[2], Minho Park[2], and Jimin Kwon[1,2] [1]Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [2]Department of Electrical Engineering, UNIST
WD1-J-6 10:30-10:45	**Energy Harvesting Performance Enhancement via Hierarchical MoS_2 Nanostructures in Triboelectric Nanogenerators** Euna Jung[1,2], Jeongin Song[1,2], Taesung Kim[2], Jae-Hyun Lee[2], and Jihun Mun[1] [1]KRISS, [2]Sungkyunkwan University

2026년 1월 28일(수), 09:00-10:45
Room E(5층, 에메랄드)

E. Compound Semiconductors 분과

O05_[WE1-E] Ultra Wide Bandgap Power Devices

좌장: 최철종 교수(전북대학교), 문재경 박사(한국전자통신연구원)

초청발표 **WE1-E-1** 09:00-09:30	**Diamond Semiconductor: From Single Crystal Wafers to Power Devices** Taemyung Kwak[1], Geunho Yoo[1], Seong-Woo Kim[2], and Okhyun Nam[1] [1]Department of Semiconductor Engineering, Tech University of Korea, [2]Orbray Co., Ltd.
WE1-E-2 09:30-09:45	**Effect of Substrate Off-Angle on the Heteroepitaxial Growth of Twin-Free (111) Diamond on Ir/r-Plane Sapphire** Seolyoung Oh, Taemyung Kwak, Yoonseok Nam, Hyunsu Ma, Geunho Yoo, and Okhyun Nam Convergence Center for Advanced Nano Semiconductor, Department of Nano-Semiconductor Engineering, Tech University of Korea
WE1-E-3 09:45-10:00	**Thermally Stable Al-rich AlGaN HEMTs for Extreme Temperature Applications** Do-Hyeong Yeo[1], Hyun-Seop Kim[2], and Ho-Young Cha[1] [1]School of Electronic and Electrical Engineering, Hongik University, [2]Department of Electrical Engineering, Kunsan National University
WE1-E-4 10:00-10:15	**Multi-Kilovolt Vertical NiO/Ga_2O_3 p-n Heterojunction Diodes with Ring-Assisted Junction Termination Extension** Kanghee Shin[1,2,3], Ho Jung Jeon[1,2,3], Jang Hyeok Park[1,2,3], and You Seung Rim[1,2,3] [1]Department of Semiconductor Systems Engineering, Sejong University, [2]Department of Convergence Engineering for Intelligent Drone, Sejong University, [3]Institute of Semiconductor and System IC, Sejong University
WE1-E-5 10:15-10:30	**NPN Gate 구조를 이용한 NiO/β-Ga_2O_3 Heterojunction Field-Effect Transistor의 게이트 안정성 및 고온 신뢰성 향상 연구** 이태은[1], 경신수[2], 우솔아[1,3] [1]국립부경대학교 지능로봇학과, [2]PowerCubeSemi, Inc., [3]국립부경대학교 전자공학과
WE1-E-6 10:30-10:45	**Characterization of Thermal Transport Properties in NiO/Ga_2O_3 p-n Junction Diode** Taeyeon Kim[1], Ho Jung Jeon[2,3], Jihyun Kim[1], You Seung Rim[2,3], and Jungwan Cho[1] [1]School of Mechanical Engineering, Sungkyunkwan University, [2]Department of Semiconductor Systems Engineering, Sejong University, [3]Department of Convergence Engineering for Intelligent Drone, Sejong University

2026년 1월 28일(수), 09:00-10:45
Room F(5층, 사파이어)

K. Memory (Design & Process Technology) 분과

O06_[WF1-K] IGZO

좌장: 홍윤기 교수(부산대학교), 곽준영 교수(이화여자대학교)

WF1-K-1 09:00-09:15	**On-Chip Trainable IGZO Analog CAM for VQ-VAE Acceleration** Hyeong Jun Seo[1,2,3], Mingi Kim[1,2,3], Youngchae Roh[1,2,3], Kanghyeon Byun[1,2,3], Changhoon Joe[1,2,3], Narae Han[1,4], Sangwook Kim[4], Sangjun Hong[5], and Sangbum Kim[1,2,3] [1]Department of Materials Science and Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University, [3]Research Institute of Advanced Materials, Seoul National University, [4]Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd., [5]Device Solutions, Samsung Electronics Co., Ltd.
WF1-K-2 09:15-09:30	**Turning the Hump into Logic: Ternary MVL via a-IGZO TFTs** Jeong Yeon Im, So-Jeong Park, Hanbin Lee, Ji Won Park, Seonghyeon Jeong, Youngmin Kim, Dae Hwan Kim, Yoon Jung Lee, and Sung-Jin Choi School of Electronics and Electrical Engineering, Kookmin University
WF1-K-3 09:30-09:45	**Back-Gate Biasing Scheme for Robust Random Access in Amorphous InGaZnO 2T0C DRAM Array with Double-Gate Structure** Seunghun Ji[1], Junsung Park[2], Hyunwook Jeong[2], Eunchong Kim[1], and Jong-Ho Bae[1] [1]Department of System Semiconductor Engineering, Yonsei University, [2]School of Electrical Engineering, Kookmin University
WF1-K-4 09:45-10:00	**Correlation between Temperature-Dependent ID-VDS Hysteresis, Schottky Barrier Non-Quasi Static Characteristics, and Trap Distribution in IGZO Vertical Channel Transistors** Jae Woo Lee[1], Wonjung Kim[1], Seong Hoon Jeon[1], Su Han Noh[1], Junseok Lee[1], Changwook Kim[1], Yoon Jung Lee[1], Sung-Jin Choi[1], Yubeen Lim[2], Min Hee Cho[2], Pilsang Yun[2], Daewon Ha[2], and Dae Hwan Kim[1] [1]School of Electrical Engineering, Kookmin University, [2]Semiconductor R&D Center, Samsung Electronics Co., Ltd.
WF1-K-5 10:00-10:15	**Analog Compute-in-Memory Transformer Using InGaZnO Charge-Trap Flash Memory** 이원주[1], 이정환[1], 구민석[2,3], 김윤[1,3] [1]서울시립대학교 전자전기컴퓨터공학과, [2]서울시립대학교 첨단융합학부, [3](주) 아이엠전자
WF1-K-6 10:15-10:30	**Enabling Selective and Tunable Weight Updates in All-InGaZnO 3-Transistor 1-Capacitor Synaptic Circuits for On-Chip Training** Minseung Kang[1,3,4], Mingi Kim[1,3,4], Jaehyeon Kang[1,2,3,4], Jongun Won[1,3,4], Hyeong Jun Seo[1,3,4], Changhoon Joe[1,3,4], Youngchae Roh[1,3,4], Yeaji Park[1,3,4], and Sangbum Kim[1,3,4] [1]Department of Materials Science and Engineering, Seoul National University, [2]Samsung Electronics Co., Ltd., [3]Inter-university Semiconductor Research Center, Seoul National University, [4]Research Institute of Advanced Materials, Seoul National University
WF1-K-7 10:30-10:45	**A Study of an OS-Based 2T0C DRAM Architecture for Buffer Using Monolithic 3D Technology** Jungho Lee and Jae Kyeong Jeong Department of Electronic Engineering, Hanyang University

2026년 1월 28일(수), 09:00-10:45
Room G(5층, 루비 II)

A. Interconnect & Package 분과

O07_[WG1-A] Advanced Package I

좌장: 이태익 수석연구원(한국생산기술연구원), 이소연 교수(인하대학교)

초청발표 **WG1-A-1** 09:00-09:30	**Single-Suppressor Cu Electrodeposition for Defect-Free TSV Filling** Myung Jun Kim School of Chemical Engineering, Sungkyunkwan University
초청발표 **WG1-A-2** 09:30-10:00	**3차원 반도체 패키지 접합용 저온 접합 소재 개발 및 신뢰성 연구** 김병준 한국공학대학교 신소재공학과
WG1-A-3 10:00-10:15	**Accurate Extraction of Ultra-Low Contact Resistivity (10^{-12} $\Omega \cdot cm^2$) via TSV-Optimized Cu-Cu Hybrid Bonding** Kyung Min Shin and Jong Kyung Park Department of Semiconductor Engineering, Seoul National University of Science & Technology
WG1-A-4 10:15-10:30	**Comparison of Signal Integrity (SI) Characteristics and Implementation of Glass and Silicon Bridge for High-Speed Interfaces** Suin Chae[1,2], Seonwoo Kim[1,3], Soobin Park[1], Se-hoon Park[1], Jaemyung Lim[2], and Jein Yu[1] [1]ICT Device Packaging Researcher Center, KETI, [2]Department of Electronic Engineering, Hanyang University, [3]School of Chemical Engineering, Sungkyunkwan University
WG1-A-5 10:30-10:45	**Novel Rinse for Fabrication of Fan-Out RDL Interposer with Embedded Bridge** Seonwoo Kim[1,2], Suin Chae[1,3], Soobin Park[1], Jein Yu[1], Sungjune Park[2], and Se-hoon Park[1] [1]ICT Device Packaging Research Center, KETI, [2]School of Chemical Engineering, Sungkyunkwan University, [3]Department of Electronic Engineering, Hanyang University

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Room H(6층, 스페이드)

G. Device & Process Modeling, Simulation and Reliability 분과

O08_[WH1-G] Device & Process Modeling, Simulation and Reliability I

좌장: 정창욱 교수(UNIST), 김현우 교수(건국대학교)

WH1-G-1 09:00-09:15	**Investigation of Bias-Dependent Off-State Leakage Current in Split-Gate VDMOS** Sung-Su Yoon, Jieun Lee, Jong Min Kim, Young Chul Kim, and Hyun Chul Nah Technology Enabling Center, DB HiTek
WH1-G-2 09:15-09:30	**Beyond the Perfect-Metal Assumption: A 3D Phase Field Simulation Framework with Thomas-Fermi Electrode Screening for FTJs** Seokwon Lee and Mincheol Shin School of Electrical Engineering, KAIST
WH1-G-3 09:30-09:45	**Accelerating Simulation of General Gate-All-Around Transistors via a Quasi-1D Model** Gyubeen Kim[1], Kwang-Woon Lee[2], and Sung-Min Hong[1,2] [1]Department of Semiconductor Engineering, GIST, [2]Department of Electrical Engineering and Computer Science, GIST
WH1-G-4 09:45-10:00	**High Performance Bi-Directional SCR with PWELL Cut-out Structure** Youngsang Son, Jongmin Kim, Youngchul Kim, and Hyunchul Nah DB HiTek
WH1-G-5 10:00-10:15	**Semi-Classical Monte-Carlo Simulation of Quantum Confinement Effects in Si Fin and Nanosheet with Different Surface Orientations** Uiho Lee, Jae Yeon Kim, and Jiwon Chang Department of System Semiconductor Engineering, Yonsei University
WH1-G-6 10:15-10:30	**A Voxel-Based Semiconductor Process Emulator, AngstromCraft** Sung-Min Hong Department of Electrical Engineering and Computer Science, GIST
WH1-G-7 10:30-10:45	**Invertible Encryption-Decryption Framework Using Threshold Switching-Based Probabilistic Bits** Jihyun Kim[1], Hyeonsik Choi[1], and Jiyong Woo[1,2] [1]School of Electronic and Electrical Engineering, Kyungpook National University, [2]School of Electronics Engineering, Kyungpook National University

2026년 1월 28일(수), 09:00-10:45
Room I(6층, 하트)

F. Silicon and Group-IV Devices and Integration Technology 분과

O09_[WI1-F] Advanced CMOS Applications

좌장: 김경록 교수(UNIST), 조성재 교수(이화여자대학교)

WI1-F-1 09:00-09:15	**Metal-Gate-Induced Stress Effects in GAAFET-Based CMOS Inverters** Subin Lim[1], Jaehyuk Lim[2], and Changhwan Shin[1] [1]School of Electrical Engineering, College of Engineering, Korea University, [2]Research Institute of Semiconductor Technology, Korea University
WI1-F-2 09:15-09:30	**Si CMOS-Compatible Ternary CMOS Technology Utilizing Intrinsic Drain-Side Resistance for Low-Power Multi-Value Logic Applications** Minsu Lim[1] and Jiwon Chang[2] [1]School of Materials Science and Engineering, Yonsei University, [2]School of System Semiconductor Engineering, Yonsei University
WI1-F-3 09:30-09:45	**Multi-Level Cell Physically Unclonable Function (PUF) based on Dual Physical Parameters in Silicon MOSFETs** Sang-Min Kang[1], Da-Eun Bang[1], Dol Sohn[1], Hyo-Jun Park[1], Eui-Cheol Yun[1], Min-Woo Kim[1], Moon-Seok Kim[2], and Jun-Young Park[1] [1]School of Semiconductor Engineering, Chungbuk National University, [2]Department of Semiconductor System Engineering, Chungnam National University
WI1-F-4 09:45-10:00	**Multi-State Probabilistic Computing Using Floating-Body MOSFETs based on the Potts Model for Solving Complex Combinatorial Optimization Problems** Sunwoo Cheong[1,2], Soo Hyung Lee[1,2], Janguk Han[1,2], and Cheol Seong Hwang[1,2] [1]Department of Materials Science and Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University
WI1-F-5 10:00-10:15	**A Study on Temporal Noise Reduction in 200Mp Pixel CMOS Image Sensors** Daehyung Lee, Hyunki Ko, Nakyung Lee, Seungjoon Lee, Kyoungeun Chang, Minkyung Kim, Kisang Yoon, Seungyeon Lee, Seunghwan Lee, Hyungchae Kim, DongHyun Kim, Jungbin Yun, and Kyungho Lee Pixel Development Team, System LSI Division, Samsung Electronics Co., Ltd.
WI1-F-6 10:15-10:30	**Efficient Phase Modulation in a Graphene-Integrated MOS Optical Phase Shifter** Gijun Ju[1,2], Kyunghwan Kim[1], Sunghyun Hwang[1], Kyul Ko[1], Yujeong Kang[1], Dae-Hwan Ahn[1], Donghee Park[1], In-Ho Lee[1], Yong-Won Song[1], Younghyun Kim[2], and Jae-Hoon Han[1] [1]Center for Quantum Technology, KIST, [2]Department of Photonics and Nanoelectronics, Hanyang University
WI1-F-7 10:30-10:45	**CMOS 공정 기반 Single-Photon Avalanche Diodes의 항복전압 및 노이즈 온도 의존성에 대한 분석** Doyoon Eom[1,2], Eunsung Park[1], Hyun-Seung Choi[1,2], Hyo-Sung Park[1], Joo-Hyun Kim[1,2], Seyoung Yook[1], Doo-Hee Son[1], Woo-Young Choi[1], and Myung-Jae Lee[1] [1]Department of Electrical and Electronic Engineering, Yonsei University, [2]Post-Silicon Semiconductor Institute, KIST

2026년 1월 28일(수), 09:00-10:30
Room J-1(6층, 다이아몬드 I)

H. Display and Imaging Technologies 분과

O10_[WJ1-H] Thin Film Transistors for Displays I

좌장: 최창순 선임연구원(KIST), 최소연 교수(한밭대학교)

WJ1-H-1 09:00-09:15	**Monolithic 3D-Integrated μLEDoS Display Using AlInP/GaInP MQW Epitaxial Layers with High Internal Quantum Efficiency and Low Size Dependence** Juhyuk Park[1], Woojin Baek[1], Hyunsu Kim[1], Dae-Myeong Geum[2], and Sanghyeon Kim[1] [1]School of Electrical Engineering, KAIST, [2]Department of Electrical & Computer Engineering, Inha University
WJ1-H-2 09:15-09:30	**Improvement of Hydrogen Resistance and Reliability in IGZO TFTs Through Nitrogen Incorporation into Al_2O_3** Sang-Hyun Kim[1], YuJin Yang[2], and Jin-Seong Park[1] [1]Department of Display Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University
WJ1-H-3 09:30-09:45	**Active-Matrix Electrochromic Monopixel Array on a Silicon Transistor Backplane** Jae Min Jeon[1], Hyo Eun Jeong[2], Jun Seo Lee[1], and Young Min Song[2] [1]School of Electrical Engineering and Computer Science, GIST, [2]School of Electrical Engineering, KAIST
WJ1-H-4 09:45-10:00	**Conformal Transfer Printing Technology on Complex Surfaces Using Shape Deformable Stamp** Hyeon Ji Yang[1], Wonseok Yang[2], and Yei Hwan Jung[1,2] [1]Department of AI Semiconductor Engineering, Hanyang University, [2]Department of Electronic Engineering, Hanyang University
초청발표 **WJ1-H-5** 10:00-10:30	**Toward Next-Generation Active-Matrix QLEDs: Optimized TFT-QLED Designs and QD Patterning Strategies** Geun Woo Baek Department of Electronic Engineering, Hanbat National University

2026년 1월 28일(수), 10:55-12:25
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O11_[WC2-D] Memory Capacitors II

좌장: 김성근 책임(KIST), 이웅규 교수(숭실대학교)

초청발표 **WC2-D-1** 10:55-11:25	**Interfacial Layer Engineering for Enhanced Properties of Scaled Memory Capacitor Materials** Dae Seon Kwon Department of Chemical and Biological Engineering, Sookmyung Women's University
WC2-D-2 11:25-11:40	**In-Situ Multimodal STEM Analysis of Interfacial Dead Layer in High-κ Oxide Thin Film Capacitors** 이기용[1], Yaolong Xing[2], 변진호[1], 정명호[3], 서진솔[4], 방정일[3], 이재호[3], 이주호[3], 김해룡[3], 이은하[3], 오상호[1] [1]한국에너지공과대학교 에너지공학부, [2]Department Structure and Nano-/Micromechanics of Materials, Max Planck Institute for Sustainable Materials, [3]삼성전자 종합기술원, [4]삼성전자 DS 부문
WC2-D-3 11:40-11:55	**High-Performance Dynamic Random Access Memory Capacitor with an Equivalent Oxide Thickness of 0.31 nm via Stepwise Cycling in Y-Doped $Hf_{0.5}Zr_{0.5}O_2$ Thin Films** Jonghoon Shin[1,2], Tae Kyun Kim[1,2], Heewon Paik[1,2], Haewon Song[1,2], and Cheol Seong Hwang[1,2] [1]Department of Materials Science and Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University
WC2-D-4 11:55-12:10	**Achieving Higher-k and Enhanced Reliability near the Morphotropic Phase Boundary in $Hf_{1-x}Zr_xO_2$ by Interfacial Nitride Metal Layer for DRAM Cell Capacitor** Jaewon Chung[1], Sangkuk Han[2], Wonjae Choi[1], Haesoo Jang[1], Kyungwook Park[2], Sangmyun Lim[1], Soyoung Park[1], Sangwoo Jeong[2], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University
WC2-D-5 12:10-12:25	**Enhancement of Fatigue Endurance in Ferroelectric $Hf_xZr_{1-x}O_2$ DRAM Capacitors through Remote Plasma ALD** Ji Won Kim, In Kook Hwang, Byung Wook Kim, Young Woon Jang, Hyeon Wu Nam, Min Kyun Kang, and Chang Bun Yoon Department of Advanced Materials Engineering, Tech University of Korea

2026년 1월 28일(수), 10:55-12:40
Room D(5층, 컨벤션홀 L)

J. Nano-Science & Technology 분과

O12_[WD2-J] 2D 반도체 기반 트랜지스터 및 디바이스

좌장: 이철호 교수(서울대학교), 강주훈 교수(연세대학교)

초청발표 **WD2-J-1** 10:55-11:25	**2D Material-Based Ferroelectric Source Gated Transistor** Joon-Seok Kim School of Electronics and Electrical Engineering, Hongik University
WD2-J-2 11:25-11:40	**P-Type Doping of Multilayer WSe_2 Transistors via Iodination** Hojun Kim, Gunwon Seo, Seongmin Lee, Danbi Lee, Jeongbin Lee, and Min Sup Choi Department of Materials Science and Engineering, Chungnam National University
WD2-J-3 11:40-11:55	**Polarity Engineering in a Single $MoTe_2$ Device for Homogeneous Complementary Circuit Applications** Hyeonchang Son[1] and Dong-Ho Kang[1,2] [1]Department of Electrical Engineering and Computer Science, GIST, [2]Department of Semiconductor Engineering, GIST
WD2-J-4 11:55-12:10	**Vertically Stacked NMOS Inverter based on Multi-layer WS_2 Formed via Multiple Wet-Transfers of Monolayer WS_2** Jiwon Ma[1], Dae Kyu Lee[2], Eunyeong Yang[1], Joon Young Kwak[3], and Jiwon Chang[1,4] [1]Department of Materials Science and Engineering, Yonsei University, [2]KIST, [3]Division of Electronic and Semiconductor Engineering, Ewha Womans University, [4]Department of System Semiconductor Engineering, Yonsei University
WD2-J-5 12:10-12:25	**A Three-Dimensional Nanogap for High-Performance MoS_2 Gate-All-Around Transistors** Junwoo Kim, Hyesu Ryu, Minjin Kim, and Sang Hyun Lee School of Chemical Engineering, Chonnam National University
WD2-J-6 12:25-12:40	**Charged Impurity-Scattering-Free Transport in Large-Area MoS_2 FETs by Diffusion-Mediated Modulation Doping** Jiwoo Yang[1,2], Yongtaek Hong[2], Takhee Lee[3,4], Kyungjune Cho[5,6], and Seungjun Chung[1] [1]School of Electrical and Engineering, Korea University, [2]Department of Electrical and Computer Engineering, Seoul National University, [3]Department of Physics and Astronomy, Seoul National University, [4]Institute of Applied Physics, Seoul National University, [5]Electronic and Hybrid Materials Research Center, KIST, [6]Convergence Research Center, KIST

2026년 1월 28일(수), 10:55-12:40
Room E(5층, 에메랄드)

E. Compound Semiconductors 분과

O13_[WE2-E] Wide Bandgap Power Devices

좌장: 이형석 기술총괄(한국전자통신연구원), 김현섭 교수(국립군산대학교)

WE2-E-1 10:55-11:10	**Normally-off Al/HfO_2/Al-Gated Diamond Field Effect Transistor on a Hetero-Epitaxially Grown Diamond Substrate** Yoonseok Nam[1], Taemyung Kwak[1], Hyunsu Ma[1], Seolyoung Oh[1], Geunho Yoo[1], Seong-Woo Kim[2], and Okhyun Nam[1] [1]Convergence Center for Advanced Nano Semiconductor, Department of Nano-Semiconductor Engineering, Tech University of Korea, [2]Orbray Co., Ltd.
WE2-E-2 11:10-11:25	**High-Temperature Reverse Bias Reliability of Edge Termination Structures in 4H-SiC Power Devices** 정승완[1], 김상엽[1], 석오균[2] [1]부산대학교 전기전자공학과, [2]부산대학교 전기전자공학부
WE2-E-3 11:25-11:40	**Enhancement-Mode Al-Rich AlGaN Channel HEMTs Realized by Superlattice and Gate Recess Design** Jaejin Heo, Joocheol Jeong, Shyam Mohan, Hyogeun Cho, Mingoo Jo, Minyeong Kim, and Okhyun Nam Convergence Center for Advanced Nano Semiconductor, Department of Nano-Semiconductor Engineering, Tech University of Korea
WE2-E-4 11:40-11:55	**상온 스퍼터링 증착 방식의 Boron Nitride를 활용한 p-GaN/AlGaN/GaN 소자 특성 향상 연구** Jun-Hyeok Yim, JinHyeok Pyo, MyeongSu Chae, SangYeon Pak, Hyungtak Kim, and Ho-Young Cha School of Electrical and Electronic Engineering, Hongik University
WE2-E-5 11:55-12:10	**Diode-Embedded E-mode P-GaN/AlGaN/GaN HEMT** Min-Ji Cho, Jun-Hyeok Lim, and Ho-Young Cha School of Electronic and Electrical Engineering, Hongik University
WE2-E-6 12:10-12:25	**Vertical GaN-Based Heterojunction Bipolar Transistors with an Al-Doped ZnO Collector** Sooyoung Kim[1,2], Go-eun Bang[3], Chang-yong Kim[3], Taenam Kwon[1], Jongseob Kim[4], Kyoung-Kook Kim[3], Dong Yeong Kim[5], and Jaehee Cho[1] [1]School of Semiconductor and Chemical Engineering, Jeonbuk National University, [2]Semiconductor Process Technology Research Center, Semiconductor Physics Research Center, Jeonbuk National University, [3]Department of Semiconductor Engineering, Tech University of Korea, [4]Samsung Electronics Co., Ltd., [5]Major of Semiconductor Engineering, Pukyong National University
WE2-E-7 12:25-12:40	**Thermal Management Solutions for GaN HEMTs through Electro-Thermal Modeling** Jisu Kim, Changhwan Song, Jungwon Choi, Hyeonjin Nam, and Jungwan Cho School of Mechanical Engineering, Sungkyunkwan University

2026년 1월 28일(수), 10:55-12:40
Room F(5층, 사파이어)

V. Quantum Technology 분과

O14_[WF2-V] Quantum Technology I

좌장: 주정진 본부장(ETRI), 최태영 교수(이화여자대학교)

초청발표 **WF2-V-1** 10:55-11:25	**Trapped Ion-Based Quantum Computing** Taeyoung Choi Department of Physics, Ewha Womans University
초청발표 **WF2-V-2** 11:25-11:55	**A Software-Defined Quantum Processor Using Neutral-Atom Arrays** 김동규 한국과학기술원 물리학과
초청발표 **WF2-V-3** 11:55-12:25	**Full-Wave 전자기 수치해석 기반의 양자 광학 현상 모델링** Dong-Yeop Na Department of Electrical Engineering, POSTECH
WF2-V-4 12:25-12:40	**Observation of PT-Symmetric Transitions in a Trapped $^{40}Ca^{+}$ Ion** Youngil Moon and Moonjoo Lee Department of Electrical Engineering, POSTECH

2026년 1월 28일(수), 10:55-12:40
Room G(5층, 루비 II)

A. Interconnect & Package 분과

O15_[WG2-A] Advanced Package II

좌장: 김명준 교수(성균관대학교), 이태익 수석연구원(한국생산기술연구원)

초청발표 **WG2-A-1** 10:55-11:25	**Comparative Study of Adhesion Energy in Symmetric and Asymmetric Substrate Bonding** Ah-Young Park[1,2] and Hakyung Jeong[3] [1]Department of Materials Science and Engineering, University of Seoul, [2]Center for Semiconductor Research, University of Seoul, [3]Semiconductor Manufacturing Research Center, KIMM
WG2-A-2 11:25-11:40	**Plasma Activated SiO_2 and SiCN Dielectrics and Bonding Characteristics** Sunbum Kim[1], Kyoungyeon Min[2], Dugkyu Han[1], Sehyeon Choi[1], Jaeho Lee[1], Kang Baek Seo[2], Ahra Jo[3], Juno Kim[3], Moonkeun Kim[3], Euisun Choi[3], and Changhwan Choi[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University, [3]Advanced Process Development Lap, Samsung Electronics Co., Ltd.
WG2-A-3 11:40-11:55	**Impact of Surface Topography on Cu/Dielectric Hybrid Bonding: A Finite Element Analysis Study** Yoonho Choi[1], So-Yeon Park[1], Minjae Park[1], Seung-Ho Seo[2], Sarah Eunkyung Kim[3], and Won-Jun Lee[1] [1]Department of Nanotechnology and Advanced Materials Engineering, Sejong University, [2]GO Element Co., Ltd., [3]Department of Semiconductor Engineering, Seoul National University of Science & Technology
WG2-A-4 11:55-12:10	**Cu-Contamination Free Hybrid Bonding via MoS_2 Passivation Layer** Hyunbin Choi[1], Sihoon Son[2,3], Dongho Lee[4], Geonwook Kim[4], and Taesung Kim[1,2,3,4] [1]Department of Semiconductor Convergence Engineering, Sungkyunkwan University, [2]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University, [3]Department of Nano Science and Technology, Sungkyunkwan University, [4]School of Mechanical Engineering, Sungkyunkwan University
WG2-A-5 12:10-12:25	**Impact of Misalignment and Dishing on Cu-Cu Hybrid Bonding Reliability** Sang-Hoon Kim[1], Changhyeon Kim[2], Jihun Kim[2], Sunwoo Han[2], Dae-Won Lee[2], Hae Ri Kim[4], Yeoun Soo Kim[4], Ji Ho Kang[4], and Eun-Ho Lee[1,2,3] [1]Department of Smart Fab. Technology, Sungkyunkwan University, [2]Department of Mechanical Engineering, Sungkyunkwan University, [3]Department of Intelligent Robotics, Sungkyunkwan University, [4]WF Bonding, SK hynix Inc.
WG2-A-6 12:25-12:40	**Epoxy-Based Reducing Polymer Composites for Low-Temperature Cu/Polymer Hybrid Bonding Processes** Dong Keon An, Chansu Jeon, and Kyung Min Kim Department of Materials Science and Engineering, KAIST

2026년 1월 28일(수), 10:55-12:40
Room H(6층, 스페이드)

G. Device & Process Modeling, Simulation and Reliability 분과

O16_[WH2-G] Device & Process Modeling, Simulation and Reliability II

좌장: 김현우 교수(건국대학교), 전종욱 교수(성균관대학교)

초청발표 **WH2-G-1** 10:55-11:25	**Quantum-Tunneling-Driven Nonradiative Carrier Trapping at Si/SiO_2 Interfaces: A First-Principles Study** Yongjin Shin Department of Semiconductor Convergence Engineering, Dankook University
WH2-G-2 11:25-11:40	**Spatial Trap Profiles in the Charge Trap Layer of 3-D NAND Flash Cell Using a Positive-Bias Induced Trap Extraction (P-BITE) Method** Seungjae Kim[1], Donghyun Go[2], Donghwi Kim[2], Daehan Won[1], and Jeong-Soo Lee[1,2] [1]Graduate School of Semiconductor Technology, POSTECH, [2]Department of Electrical Engineering, POSTECH
WH2-G-3 11:40-11:55	**Dynamic Source-resistance in RF GaN HEMTs and Its Impact on the g_m Non-linearity** Su-Min Choi[1], Wan-Soo Park[1], Min-Gyu Song[1], Se-Hun Kim[1], Ji-In Byeon[1], Seung-Woo Son[1], In-Geun Lee[1], Ho-Kyun Ahn[2], Dong-Hee Shin[3], Young-Kyun Noh[3], Jae-Hak Lee[1], Kyounghoon Yang[4], and Dae-Hyun Kim[1] [1]Kyungpook National University, [2]ETRI, [3]IVWorks Co., Ltd., [4]KAIST
WH2-G-4 11:55-12:10	**Accuracy Test of Numerical Methods for Generalization of Scharfetter-Gummel Scheme** Ji-Young Kim and Sung-Min Hong Department of Electrical Engineering and Computer Science, GIST
WH2-G-5 12:10-12:25	**Investigation of Threshold Voltage Instability in E-Mode GaN HEMTs through TCAD Simulations** Geon-Tae Jang, Nakwon Yu, Jongmin Kim, Youngchul Kim, and Hyunchul Nah Technology Enabling Center, DB HiTek
WH2-G-6 12:25-12:40	**Characterization of Well Proximity Effect and TCAD Calibration for CIS Pixel Implant** Kyeongjin Park, Jongmin Kim, Youngchul Kim, and Hyunchul Nah Korea Tech. Enabling Center, DB HiTek Co. Ltd

2026년 1월 28일(수), 10:55-12:40
Room I(6층, 하트)

F. Silicon and Group-IV Devices and Integration Technology 분과

O17_[WI2-F] Special Topics: Device Reliability/Annealing Process

좌장: 김상완 교수(서강대학교), 김경록 교수(UNIST)

초청발표 **WI2-F-1** 10:55-11:25	**Introduction to Rad-hardened Semiconductor R&D and Test Infra for Aero-space Application** Chang Goo Kang, Jeong Min Park, Su Jin Kim, and Yongsu Lee Advanced Radiation Technology Institute, KAERI
초청발표 **WI2-F-2** 11:25-11:55	**RGB Continuous-Wave Laser Annealing for Low Thermal Budget CMOS Integration: Junction Activation, Silicidation and Ferroelectric HZO Crystallization** Hyeon Jun Hwang Department of Semiconductor Engineering, Mokpo National University
WI2-F-3 11:55-12:10	**Comparative Study of Multiple High-Pressure Rapid Deuterium Annealing for MOSFET Performance Enhancement** Min-Woo Kim, Hyo-Jun Park, Eui-Cheol Yun, Sang-Min Kang, Da-Eun Bang, Dol Sohn, and Jun-Young Park School of Semiconductor Engineering, Chungbuk National University
WI2-F-4 12:10-12:25	**Process Optimization for Highly Activated Ultra-Shallow Junction Formation with Continuous Wave Laser Annealing** Gunryeol Cho, Sanguk Lee, Yonghwan Ahn, Minchan Kim, Sunmin Yeou, Jaeseong Pyo, Jitae Yoo, and Rock-Hyun Baek Department of Electrical Engineering, POSTECH
WI2-F-5 12:25-12:40	**Mitigating BTI Degradation in HKMG Transistors via Oxygen Reservoir Layer Engineering** Kyungwook Park[1,3], Sangkuk Han[1], Wonjae Choi[2], Haesoo Jang[2], Jaewon Chung[2], Sangmyun Lim[2], Sangwoo Jeong[1], Soyoung Park[2], and Changhwan Choi[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University, [3]DRAM Process Development Team, Samsung Electronics Co., Ltd.

2026년 1월 28일(수), 10:55-12:40
Room J-1(6층, 다이아몬드 I)

H. Display and Imaging Technologies 분과

O18_[WJ2-H] Photodiodes and Image Sensors

좌장: 백근우 교수(한밭대학교), 최창순 선임연구원(KIST)

초청발표 **WJ1-H-1** 10:55-11:25	**Wide Bandgap Semic[illegible]Photomemory Application** Ramit Kumar Mondal, Y[illegible]n School of Electrical and Electronic Engineering, Nanyang Technological University
WJ2-H-2 11:25-11:40	**Single-Band Guided-Mode Resonance InGaAs Photodetector for Multispectral Polarization Sensing** Junho Jang[1], Il-Suk Kang[2], Yeon-Wha Oh[2], Sanghee Jung[2], Huijae Cho[2], and SangHyeon Kim[1] [1]School of Electrical Engineering, KAIST, [2]NNFC
WJ2-H-3 11:40-11:55	**Hyperspectral Imaging via Air-Gap Cavity Tunable Filter** Nayeon Kim[1,2], Sunghyun Hwang[1], Eui-Hyoun Ryu[1], Ji-Hwan Son[1], Nayoung Kim[1], and In-Ho Lee[1] [1]Center for Quantum Technology, KIST, [2]School of Electrical Engineering, Korea University
WJ2-H-4 11:55-12:10	**Ultra Low Noise Global Shutter CMOS Image Sensor with High Density MIM Capacitor** Junha Kang, Yoonjay Han, Taemin Kim, Jonguk Kim, Suji Hwang, Jihye Jeong, Jungsan Kim, Sangjin Choi, Yongsoon Park, Daekun Ahn, Jae-Kyu Lee, and Jonghyun Go Semiconductor R&D Center, Samsung Electronics Co., Ltd.
WJ2-H-5 12:10-12:25	**Pixel-like TEG Design for Accurate FD-Leakage Prediction in Global-Shutter CIS Sensors** Surim Lee, Jaehoon Jeon, Haeyong Park, Jeong-soon Kang, Sangyoon Kim, Jaehyun Kim, Taehyung Kim, Woochan Lee, Seung-Sik Kim, Jae-Kyu Lee, and Jonghyun Go Semiconductor R&D Center, Samsung Electronics Co., Ltd.
WJ2-H-6 12:25-12:40	**최첨단 High CRA CIS의 Gr Gb Difference 원인 분석** 강정우[1], 황제혁[1], 박민영[3], 정재오[3], 추성민[3], 김동수[3], 이지원[1,2] [1]포항공과대학교 반도체대학원, [2]포항공과대학교 반도체공학과, [3]삼성전자 MX사업부

철 회

2026년 1월 28일(수), 16:00-17:30
Room A(4층, 그랜드볼룸 I+II)

M. RF and Wireless Design 분과

O19_[WA3-M] RF and Wireless Design

좌장: 권구덕 교수(강원대학교), 김주성 교수(이화여자대학교)

초청발표 **WA3-M-1** 16:00-16:30	**Low Noise and Broadband Cryo-CMOS Receiver for Superconducting Multi-qubits Read-out** Jusung Kim[1], Hyeonsik Ahn[2], Juhui Jeong[3], and Junghwan Han[3] [1]Division of Electronic and Semiconductor Engineering, Ewha Womans University, [2]Department of Electronics Engineering, Hanbat National University, [3]Department of Radio and Information Communication Engineering, Chungnam National University
WA3-M-2 16:30-16:45	**Channel-Selection LNA with Complex Pole *N*-Path Feedforward Blocker Cancellation for Advanced 5G NR FDD RX** Hyeonjun Kim, Sengjun Jo, and Kuduck Kwon Department of Electronic Engineering, Kangwon National University
WA3-M-3 16:45-17:00	**HM3D Integrated RF Platform with III-V HEMTs on Si CMOS for Next-Generation Wireless Communication Systems** Jaeyong Jeong[1], Jeong-Taek Lim[2], Yoon-Je Suh[1], Nahyun Rheem[1], Chan Jik Lee[1], Bong Ho Kim[3], Joon Pyo Kim[3], Jongmin Kim[4], Jongwon Lee[5], Choul-Young Kim[2], and Sanghyeon Kim[1,6] [1]School of Electrical Engineering, KAIST, [2]Department of Electronics Engineering, Chungnam National University, [3]Samsung Electronics Co., Ltd., [4]KANC, [5]Department of Semiconductor Convergence, Chungnam National University, [6]Graduate School of Semiconductor Technology, KAIST
초청발표 **WA3-M-4** 17:00-17:30	**A Fully Integrated IEEE 802.15.4/4z-Compliant IR-UWB System-on-Chip RF Transceiver Supporting Precision Positioning and Channels 5 to 12** Sinyoung Kim, Hyun-Gi Seok, and Hyun-Chul Park System LSI Division, Samsung Electronics Co., Ltd.

2026년 1월 28일(수), 16:00-17:30
Room B(4층, 그랜드볼룸 III)

K. Memory (Design & Process Technology) 분과

O20_[WB3-K] Advanced Memory

좌장: 강명곤 교수(서울시립대학교), 백승재 마스터(삼성전자)

초청발표 **WB3-K-1** 16:00-16:30	**AI-Driven Device and Process Modeling Platforms for Next-Generation Semiconductor Development** Hyunbo Cho Alsemy Inc.
WB3-K-2 16:30-16:45	**Block-Diagonal Hadamard Matrices Based Dynamic Transfer Algorithm for Volatile Processing-In-Memory Based Cross-Point Arrays** Jinho Byun[1], Sengkun Kim[2], Jeonghoon Son[1], and Seyoung Kim[1,3] [1]Department of Electrical Engineering, POSTECH, [2]Department of Materials Science and Engineering, POSTECH, [3]Graduate School of Semiconductor Technology, POSTECH
WB3-K-3 16:45-17:00	**Self-Rectifying Characteristics in RRAM Using Semiconducting CNT Selector Layer** Chan-Hyeok Nam[1], Be[illegible] Jo[1], Beom Joon Jung[1], Ju Han Ryu[2], Yeongmyeong Cho[2], Sang Min Park[2], Goeun Heo[2], Younglae [illegible] [1]Department of Electro[illegible] University, [2]Department of Electronic and Semiconductor Engineering, Gangneung-Wonju National University
WB3-K-4 17:00-17:15	**A Configurable Processing-in-Memory Evaluation Framework for Large Language Model Inference** Minki Choi, Juhyeon Lee, and Wonbo Shim Department of Electrical and Information Engineering, Seoul National University of Science & Technology
WB3-K-5 17:15-17:30	**A Partially-Unrolled DFE Architecture for Low-Power, Low-Area High-Speed DSP Receivers** Seung Yun Lee and Jaeha Kim Department of Electrical and Computer Engineering, Seoul National University

철 회

2026년 1월 28일(수), 16:00-17:30
Room J-2(6층, 다이아몬드 II)

I. MEMS & Sensors Systems 분과

O21_[WJ3-I] MEMS and Sensor System I

좌장: 박윤석 교수(경희대학교), 최준환 교수(단국대학교)

초청발표 **WJ3-I-1** 16:00-16:30	**Electromechanical and Electrochemical Energy Harvesting from Ambient Moisture** Jiaming Zhou, Eunjong Kim, and Dong-Myeong Shin Department of Mechanical Engineering, The University of Hong Kong
WJ3-I-2 16:30-16:45	**Radiation Hardness of Graphene Gas Sensor** Jaeyeon Oh[1,2], Jongin Park[1], and Yeonhoo Kim[1] [1]Strategic Technology Research Institute, KRISS, [2]Department of Materials Science and Engineering, Seoul National University
WJ3-I-3 16:45-17:00	**High-Sensitivity Pressure Sensors based on 3D Hierarchical MoS_2 with Wide Dynamic Range** Jeongin Song[1,2], Se Min Hwang[1,3], Min Sup Choi[3], Sang Woo Kang[1,4], Taesung Kim[2], and Jihun Mun[1] [1]Semiconductor and Display Metrology Group, KRISS, [2]School of Mechanical Engineering, Sungkyunkwan University, [3]Department of Materials Science and Engineering, Chungnam National University, [4]Measurement Engineering, University of Science and Technology
초청발표 **WJ3-I-4** 17:00-17:30	**On-Device AI Sensors: Gaussian Transistors and Light-Driven Spikes for Deepfake Detection** Hocheon Yoo Department of Electronic Engineering, Hanyang University

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Room D(5층, 컨벤션홀 L)

R. Semiconductor Software 분과

O22_[WD3-R] R & O 분과 통합 세션 (부제: Semiconductor Software)

좌장: 강동현 교수(동국대학교), 최웅 교수(숙명여자대학교)

초청발표 **WD3-R-1** 16:00-16:30	**High Accuracy Reverse Engineering Tool for Xilinx FPGAs** Soyeon Choi Department of Semiconductor System Engineering, Hanbat National University
초청발표 **WD3-R-2** 16:30-17:00	**Toward 100M IOPS SSD in the AI Era** Eyee Hyun Nam FADU Inc.
WD3-R-3 17:00-17:15	**Bottleneck Analysis of On-Device Large Language Model Inference under Out-of-Core Execution** Seunghun Oh and Jisung Park Department of Computer Science and Engineering, POSTECH
WD3-R-4 17:15-17:30	**eBPF를 활용한 Linux 커널 I/O 스택의 계층별 지연 시간 분석** 김유리[1], 이찬용[2], 강동현[1] [1]동국대학교 컴퓨터·AI학부, [2]동국대학교 일반대학원 컴퓨터·AI학과

2026년 1월 28일(수), 16:00-17:15
Room E(5층, 에메랄드)

E. Compound Semiconductors 분과

O23_[WE3-E] High Speed Devices and Circuits

좌장: 김형탁 교수(홍익대학교), 고유민 실장(한국나노기술원)

WE3-E-1 16:00-16:15	**f_T = 815 GHz $In_{0.8}Ga_{0.2}As/In_{0.52}Al_{0.48}As$ QW HEMTs with L_g = 23 nm** Seung-Woo Son[1], Min-Seo Yu[1], Sang-Pyeong Son[1], In-Geun Lee[1], Kyounghoon Yang[2], Jae-Hak Lee[1], and Dae-Hyun Kim[1] [1]School of Electronic and Electrical Engineering, Kyungpook National University, [2]KAIST
WE3-E-2 16:15-16:30	**Effect of a Wider Bandgap Al-Rich InAlAs Layer on Suppressing Gate Leakage in Low-Noise InP HEMTs** Juwon Seo[1,2], Won Jun Lee[1,3], Il Ki Han[1], DaeHwan Ahn[4], Jae-Hoon Han[4], Mun Seok Jeong[2], and JoonHyun Kang[1] [1]Nanophotonic System Research Center, KIST, [2]Department of Physics, Hanyang University, [3]School of Electrical Engineering, Korea University, [4]Center for Quantum Technology, KIST
WE3-E-3 16:30-16:45	**InAlGaN/AlN/GaN High-electron Mobility Transistors with Selective n+ GaN S/D Regrowth and f_T 〉 250 GHz** Wan-Soo Park[1], Su-Min Choi[1], Min-Gyu Song[1], Se-Hun Kim[1], Ji-In Byeon[1], Seung-Woo Son[1], In-Geun Lee[1], Ho-Kyun Ahn[2], Dong-Hee Shin[3], Young-Kyun Noh[3], Jae-Hak Lee[1], Kyounghoon Yang[4], and Dae-Hyun Kim[1] [1]Kyungpook National University, [2]ETRI, [3]IVWorks Co., Ltd., [4]KAIST
WE3-E-4 16:45-17:00	**Heterogeneous 3D Integrated RF Platform on CMOS via Die-to-Wafer Bonding Technology** Jaeyong Jeong[1], Chan Jik Lee[1], Yoon-Je Suh[1], Nahyun Rheem[1], Bong Ho Kim[1,2], Joon Pyo Kim[1,2], Juhyuk Park[1], and Sanghyeon Kim[1,3] [1]School of Electrical Engineering, KAIST, [2]Samsung Electronics Co., Ltd., [3]Graduate School of Semiconductor Technology, KAIST
WE3-E-5 17:00-17:15	**Heterogeneous InGaAs/InP Biristor Oscillators for Fast, Power-Efficient Ising Machine Hardware** 이현준[1], 김준표[2,3], 김상현[1,2] [1]KAIST 반도체공학대학원, [2]KAIST 전기 및 전자공학부, [3]삼성전자 반도체연구소

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Room F(5층, 사파이어)

C. Material Growth & Characterization 분과

O24_[WF3-C] Functional Membranes, Sensing, and Advanced Characterization

좌장: 김태헌 책임박사(KIST), 손창희 교수(UNIST)

초청발표 **WF3-C-1** 16:00-16:30	**Freestanding Single-crystalline Membranes in Chemical Sensor Application** Jun Min Suh[1,2] [1]School of Transdisciplinary Innovations, Seoul National University, [2]Department of Materials Science and Engineering, Seoul National University
WF3-C-2 16:30-16:45	**Epitaxial Growth of Wurtzite BeO on Corundum α-Ga_2O_3 via Plasma-Enhanced Atomic Layer Deposition for Wide-Bandgap Power Devices** Jonghyun Bae[1,2], Dohwan Jung[1], Haekyun Bong[1,2], Hyeong-Yun Kim[3], Ji-Hyeon Park[3], Dae-Woo Jeon[3], and Jungwoo Oh[1,2] [1]School of Integrated Technology, Yonsei University, [2]BK21 Graduate Program in Intelligent Semiconductor Technology, Yonsei University, [3]KICET
WF3-C-3 16:45-17:00	**High Thermal Conductivity of Sub-100 nm BeO Thin Films** Jihyun Kim[1], Jonghyun Bae[2,3], Jisu Kim[1], Dohwan Jung[2], Dongyun Seo[1], Jungwoo Oh[2,3], and Jungwan Cho[1] [1]School of Mechanical Engineering, Sungkyunkwan University, [2]School of Integrated Technology, Yonsei University, [3]BK21 Graduate Program in Intelligent Semiconductor Technology, Yonsei University
WF3-C-4 17:00-17:15	**Deep Learning Analysis of 4D-STEM Reveals 3D Polarization and Switching in Ferroelectric Capacitors** Jinho Byun[1], Keeyong Lee[1], Jeongil Bang[2], Jaeho Lee[2], Jooho Lee[2], Haeryoung Kim[2], Geun Ho Gu[1], and Sang Ho Oh[1] [1]Department of Energy Engineering, KENTECH, [2]Thin Film TU, Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd.
WF3-C-5 17:15-17:30	**Direct Synthesis of Surface Functional Group-free Molybdenum Carbide MXene Thin Films by Chemical Vapor Deposition for Nitrogen Reduction Reaction** Junhyeok No[1], Taemin Ahn[2], Tae Hwan Kim[3], and Hee Cheul Choi[1,4] [1]Division of Advanced Materials Science, POSTECH, [2]Pohang Accelerator Laboratory, POSTECH, [3]Department of Physics, POSTECH, [4]Department of Chemistry, POSTECH

2026년 01월 28일(수), 16:00-17:00
Room G(5층, 루비 II)

S. Chip Design Contest 분과

O25_[WG3-S] Chip Design Contest

좌장: 조경록 교수(충북대학교), 양종렬 교수(건국대학교)

WG3-S-1 16:00-16:15	**An 850μW, 2-to-5GHz Jitter-Filtering and Instant-Toggling Injection-Locked Quadrature-Clock Generator for Low-Power Clock Distribution in HBM Interfaces** Jeongbeom Seo[1], Yuhwan Shin[2], and Jaehyouk Choi[1] [1]Department of Electrical and Computer Engineering, Seoul National University, [2]Electrical Engineering, KAIST
WG3-S-2 16:15-16:30	**A 0.4-VDDQ 11.5-Gb/s/pin Transmitter with Switched-Coupling Charge-Pump Crosstalk Cancellation Achieving Eye-Margin Recovery for Ultra-Dense Die-to-Die Interfaces** Yoochang Kim[1] and Young-Ha Hwang[1,2] [1]Department of Intelligent Semiconductors, Soongsil University, [2]School of Electronic Engineering, Soongsil University
WG3-S-3 16:30-16:45	**Small-Area, High-Speed, and High Uniformity Source Driver IC for OLED-on-Silicon (OLEDoS) Displays** Jung Hwan Oh, Wi Man Yoo, Dong Kun Lee, and Jong Seok Kim Department of Electronics and Electrical Engineering, Hanyang University ERICA
WG3-S-4 16:45-17:00	**An Energy-Efficient Multi-Cell Battery Charger with Simultaneous Charging and Balancing** Seongil Yeo and Kunhee Cho Department of Semiconductor Convergence Engineering, Sungkyunkwan University

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Room H(6층, 스페이드)

G. Device & Process Modeling, Simulation and Reliability 분과

O26_[WH3-G] Device & Process Modeling, Simulation and Reliability III

좌장: 권용우 교수(홍익대학교), 김병조 교수(UNIST)

초청발표 **WH3-G-1** 16:00-16:30	**Bridging Atomistic Kinetics and Fluid Dynamics: A Multiscale Simulations from DFT Integrated Transient CFD for Industrial-Scale Spatial ALD** Hwanyeol Park[1,2] [1]Department of Display Materials Engineering, Soonchunhyang University, [2]Department of Electronic Materials, Devices, and Equipment Engineering, Soonchunhyang University
WH3-G-2 16:30-16:45	**Impact of Power Cycling Test on the Electrical Characteristics of p-GaN HEMTs** Taehyeon Kim[1,2], Kihyun Kim[1], Sungsik Lee[2], and Inho Kang[1] [1]Power SoC Research Center, KERI, [2]Department of Electronic Engineering, Pusan National University
WH3-G-3 16:45-17:00	**Analysis of Quasi-Bound-State Tunneling in AlGaN/AlN/GaN HEMTs by NEGF-Based Quantum Transport Approach** Heonseok Oh and Mincheol Shin School of Electrical Engineering, KAIST
WH3-G-4 17:00-17:15	**TCAD Framework for Predicting Breakdown Voltage, Photon Detection Probability, and Dark Count Rate in Single-Photon Avalanche Diodes** Nakwon Yu, Jongmin Kim, Youngchul Kim, Ju-Hwan Jung, Sanghwan Kim, Man-Lyun Ha, and Hyunchul Nah Technology Enabling Center, DB HiTek
WH3-G-5 17:15-17:30	**Investigation of Cell-to-Cell Analysis Methodology for ESD Protection Devices Using TCAD Simulation** Jehoon Lee, Jongmin Kim, and Youngchul Kim Technology Development Department, DB HiTek

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Room I(6층, 하트)

F. Silicon and Group-IV Devices and Integration Technology 분과

O27_[WI3-F] Memory and Logic Devices for AI

좌장: 정규원 교수(서울대학교), 김시현 교수(서강대학교)

WI3-F-1 16:00-16:15	**Hopfield Neural Networks Using Vertical NAND Flash Memory for Large-Scale In-Memory Associative Computing** Jin Ho Chang[1,2], Jae Seung Woo[1,2], Suk-Kang Sung[3], Ki-Whan Song[4], and Woo Young Choi[1,2] [1]Department of Electrical and Computer Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University, [3]Advanced Flash Technology Team, Samsung Electronics Co., Ltd., [4]Flash Design Team, Samsung Electronics Co., Ltd.
WI3-F-2 16:15-16:30	**Automatic Training of Reconfigurable Analog Logic Circuit via LTSPICE-Python Co-Simulation towards Accuracy Maximization** Jooeun Lee[1,2] and Seongjae Cho[1,2] [1]Division of Electronics and Semiconductor Engineering, Ewha Womans University, [2]Institute for Multiscale Matter and Systems (IMMS), Ewha Womans University
WI3-F-3 16:30-16:45	**Comparative Analysis of Channel Materials and Device Architectures in 2T0C DRAM** Jimin Son and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University
WI3-F-4 16:45-17:00	**Bonding Pressure Annealing Technique to Improve Reliability of FeRAM** Myeongjae Choi[1], Chaeho Kwon[2], Jeongheon Cho[2], and Changhwan Shin[3] [1]Department of Semiconductor System Engineering, Korea University, [2]Department of Semiconductor Engineering, Korea University, [3]School of Electrical Engineering, College of Engineering, Korea University
WI3-F-5 17:00-17:15	**Analysis on High-Frequency Capacitance Characteristics of Si-Compatible Dual-Layer RRAM Designed for Low-Power Applications** Euni Ko[1,2], Soomin Kim[1,2], and Seongjae Cho[1,2] [1]Department of Semiconductor Engineering, Ewha Womans University, [2]Institute for Multiscale Matter and Systems (IMMS), Ewha Womans University
WI3-F-6 17:15-17:30	**Via-embedded Self-rectifying Memristor based on 180nm CMOS Process** Solji Park[1], Gapseop Sim[2], Won-Chul Lee[2], Woo-Suk Sul[2], Kyung Min Kim[3], and Jongwon Lee[1] [1]Chungnam National University, [2]NNFC, [3]KAIST

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Room J-1(6층, 다이아몬드 I)

T. AI 분과

O28_[WJ3-T] Artificial Intelligence II

좌장: 박정우 교수(성균관대학교), 김병수 센터장(KETI)

초청발표 **WJ3-T-1** 16:00-16:30	**Ultra-low Power LLM Processor with Binary/Ternary Quantization** Sangyeob Kim School of Integrated Technology, Yonsei University
WJ3-T-2 16:30-16:45	**Deep Q-Network 기반 온-디바이스 자율주행로봇 경로 도출 시스템** 권은혜, 백돈규 충북대학교 반도체공학부
WJ3-T-3 16:45-17:00	**Compute-in-Memory 구조 기반 근전도 신호 획득 및 손동작 분류 System-on-Chip** 홍준성[1,3], 유희재[1,3], 구민석[2,3,4], 김윤[1,3,4] [1]서울시립대학교 전자전기컴퓨터공학과, [2]서울시립대학교 첨단융합학부, [3]서울시립대 반도체 연구센터(UOS-FAB), [4]주식회사 IM전자
WJ3-T-4 17:00-17:15	**BF16-to-BFP Conversion Architecture for Systolic Array Computation** Jihyeon Hwang, Taehong Min, Jungwoo Park, and Seung Eun Lee Department of Electronic Engineering, Seoul National University of Science & Technology
WJ3-T-5 17:15-17:30	**Low-Latency and Resource-Optimized LeNet-5 Accelerator Using FPGA** DongHwan Yoon, JoonSeok Kim, and Seokhyeong Kang Graduate School of Semiconductor Technology, POSTECH

2026년 1월 29일(목), 09:00-10:45
Room A(4층, 그랜드볼룸 I+II)

D. Thin Film Process Technology 분과

O29_[TA1-D] Emerging Devices I

좌장: 최병준 교수(서울과학기술대학교)

초청발표 **TA1-D-1** 09:00-09:30	**Resistive Switching Materials and Devices for Information Processing** Kyung Seok Woo[1,2] [1]Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [2]Department of Materials Science and Engineering, UNIST
TA1-D-2 09:30-09:45	**Li Doped NbO_x Self-Rectifying Memristors for Crossbar Array Neuromorphic Architectures** Jeong Hyeon Son and Hong-Sub Lee Department of Materials Science and Engineering, Kyung Hee University
TA1-D-3 09:45-10:00	**Two-Stack 2k-Level Crossbar Array based on Alkali-Ion Al:TiO_2 Memristors** Dae Hee Han and Hong Sub Lee Department of Advanced Materials Engineering, Kyung Hee University
TA1-D-4 10:00-10:15	**Tuning Switching Dynamics in ZnO Transistors with TiO_2 Memristor Gates for Neuromorphic Computing** Yun Seo Shin and Hong Sub Lee Department of Advanced Materials Engineering, Kyung Hee University
TA1-D-5 10:15-10:30	**Li-well ZnO Memtransistors Cross-bar Array for Neuromorphic Applications** Hyun Sik Kim, Ki Hoon Son, and Hong Sub Lee Department of Advanced Materials Engineering for Information and Electronics, Kyung Hee University
TA1-D-6 10:30-10:45	**Analysis of Switching Characteristics and Thermal Stability in 2DEG-Based Conductive-Bridge Random Access Memory** In Su Oh[1,2], Ju Young Sung[1,2], Chae Hyun Lee[1,2], Ye Bin Lim[1,2], Sang Hyeok Lee[1,2], Yun Won Song[1,2], and Sang Woon Lee[1,2] [1]Department of Energy Systems Research, Ajou University, [2]Department of Physics, Ajou University

2026년 1월 29일(목), 09:00-10:45
Room B(4층, 그랜드볼룸 III)

B. Patterning (Lithography & Etch Technology) 분과

O30_[TB1-B] Patterning (Lithography)

좌장: 정현담 교수(전남대학교), 김명웅 교수(인하대학교)

초청발표 **TB1-B-1** 09:00-09:30	**Eco-Friendly Water-Processable Dual-Tone Photoresists Containing Photoreversible Functional Groups for Advanced Lithography** Hyun-Jin Kim[1], Min-Jung Park[1], Gayoung Kim[2], Jin-Kyun Lee[2], and Jae-Hak Choi[1] [1]Department of Materials Science and Engineering, Chungnam National University, [2]Program in Environment and Polymer Engineering, Inha University
TB1-B-2 09:30-09:45	**이미징 성능 및 Best Focus Shift 완화를 위한 High-NA EUV 마스크용 Bilayer 흡수체 구조 연구** 이승호[1,2], 정동민[1,2], 김연수[1,2], 이태호[2], 안진호[1,2] [1]한양대학교 신소재공학과, [2]극한스케일·극한물성-이종집적 한계극복 반도체 기술 연구센터
TB1-B-3 09:45-10:00	**Simulation of Extreme Ultraviolet Mask for Defect Inspection and Repair** Sang-Kon Kim Hongik University
TB1-B-4 10:00-10:15	**Grain Size에 따른 EUV 펠리클의 기계적 및 광학적 특성 변화** 김원진[1,2], 강영우[1,2], 이태호[1,2], 박영욱[2], 안진호[1,2] [1]한양대학교 신소재공학과, [2]극한스케일·극한물성-이종집적 한계극복 반도체 기술 연구센터
TB1-B-5 10:15-10:30	**A Methodology of Emissivity Measurement for Radiatively Complex CNT and Porous-Structured Pellicles** Jiho Kim[1], Youngchan Kim[3], Hyun Don Kim[3], Hyeongjoon Lim[3], Hyuk Jin Kim[1], Geonhwa Kim[1], Boknam Chae[1], Eunjip Choi[3], and Sangsul Lee[1,2] [1]Pohang Accelerator Laboratory, POSTECH, [2]Department of Semiconductor Engineering, POSTECH, [3]Department of Physics, University of Seoul
TB1-B-6 10:30-10:45	**Gap-filling Stencil Lithography Utilizing Protective Layer for Precise Patterning of 2D Transition-metal Dichalcogenide Electronics** Jaemin Myoung[1,2,3], Taehyeon Kim[1,2,3], Seunghun Lee[4], Jeonghwan Kim[4], Taesung Kim[5], and Jihun Mun[1] [1]Strategic Technology Research Institute, KRISS, [2]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University, [3]Department of Nano Science and Technology, Sungkyunkwan University, [4]Department of Materials Science & Engineering, Hanbat National University, [5]School of Mechanical Engineering, Sungkyunkwan University

2026년 1월 29일(목), 09:00-10:45
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O31_[TC1-D] Ferroelectrics I

좌장: 엄태용 교수(세종대학교), 박민혁 교수(서울대학교)

초청발표 **TC1-D-1** 09:00-09:30	**Advanced Synchrotron-Based X-ray Diffraction Characterization of Ferroelectric HfO_2 for Emerging Memory Applications** Younghwan Lee[1] and Min Hyuk Park[2] [1]School of Materials Science and Engineering, Chonnam National University, [2]Department of Materials Science and Engineering, Seoul National University
TC1-D-2 09:30-09:45	**Antiferroelectric Shift of $Hf_{0.2}Zr_{0.8}O_2$ Thin Film Capacitors via NbC Low-Work Function Transition Metal Electrodes** Kwan Hyun Park[1], Chae Hyun Park[2], Soo Hyun Kim[2], and Min Hyuk Park[1] [1]Department of Materials Science and Engineering, Seoul National University, [2]Department of Materials Science and Engineering, UNIST
TC1-D-3 09:45-10:00	**A Study on the Role of O_2 Plasma-Controlled TiOx Interfacial Layer for Reliability Enhancement of HZO Ferroelectric Capacitors** So Yeong Park, Woon San Ko, Hye Ri Hong, Seong Jo Jo, and Ga Won Lee School of Electronics Engineering, Chungnam National University
TC1-D-4 10:00-10:15	**Stable Ferroelectric Properties in 3 nm Hafnium-Zirconium-Oxide Thin Films by Shifting the Composition Window** Gunho Kim[1], Hyo-Bae Kim[1], Wonwoo Kho[2], Hye Won Cho[1], Hyung-Seok Lee[1], Seung-Eon Ahn[3], and Ji-Hoon Ahn[1] [1]Department of Materials Science & Chemical Engineering, Hanyang University, [2]Department of IT · Semiconductor Convergence Engineering, Tech University of Korea, [3]Department of Nano & Semiconductor Engineering, Tech University of Korea
TC1-D-5 10:15-10:30	**Polarization Characteristics of Nano-Laminated Thick $Hf_{0.5}Zr_{0.5}O_2$ with Al_2O_3 Interlayer** Yu-Jeong Kang[1,2], Kyul Ko[1], Woo-Young Choi[2], and Jae-Hoon Han[1] [1]Center for Quantum Technology, KIST, [2]Department of Electrical and Electronic Engineering, Yonsei University
TC1-D-6 10:30-10:45	**Enhanced Thermal Robustness of $Hf_xZr_{1-x}O_2$ through Lanthanum Oxygen Diffusion Interlayer** Jihoon Choi[1], KyungSoo Park[2], HyeonCheol Jeong[1], SangMyum Lim[1], TaeSuk Kim[2], GyuMin Hwang[1], YeonWoo Choi[1], JinYeong Lee[1], YoonSeok Lee[1], YeJun Park[1], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University

2026년 1월 29일(목), 09:00-10:45
Room D(5층, 컨벤션홀 L)

K. Memory (Design & Process Technology) 분과

O32_[TD1-K] NAND Flash

좌장: 박종경 교수(서울과학기술대학교), 전종욱 교수(성균관대학교)

초청발표 **TD1-K-1** 09:00-09:30	**Evolution of Device Technology for Next Generation VNAND** Kibong Moon Flash TD Team, Semiconductor R&D Center, Samsung Electronics Co., Ltd.
TD1-K-2 09:30-09:45	**Implementation of n-Shot STDP Pulse Scheme for Flash Memory Array-Based Low-Power SNN** Jaewon Kim[1], Jangsaeng Kim[1,2], and Jong-Ho Bae[3] [1]Department of Elect … [2]Department of System Semiconductor Engineering, Sogang U … nductor Engineering, Yonsei University
TD1-K-3 09:45-10:00	**Improved Surrogate Learning of Threshold-Voltage Distribution in 3D NAND Flash Using Ensemble-Driven MLP Optimization** Hyeon Seo Yun and Jong Kyung Park Department of Semiconductor Engineering, Seoul National University of Science & Technology
TD1-K-4 10:00-10:15	**Low-Power, Area-Efficient NAND-AND Hybrid Flash MCAM for High-Density In-Memory Search** Seoung Youl Lee[1,2], Sung Yun Woo[3], and Dongseok Kwon[2] [1]Department of Electrical and Electronic Engineering, Inha University, [2]Department of Semiconductor Engineering, GIST, [3]School of Electronics Engineering, Kyungpook National University
TD1-K-5 10:15-10:30	**고성능 낸드 플래시 메모리를 위한 iCVD 공정 기반 다결정 실리콘 채널 내 불소 도핑 기술 개발** 박영근[1], 박정익[2], 정재중[1], 장성진[3], 박세준[4], 임성갑[2], 조병진[1] [1]한국과학기술원 전기 및 전자공학부, [2]한국과학기술원 생명화학공학과, [3]나노종합기술원, [4]삼성전자
TD1-K-6 10:30-10:45	**Analog Compute-In-Memory based on Flash Memory Cells for Hopfield Neural Networks** Yoosung Jeon[1,2] and Dongseok Kwon[2] [1]Department of Materials Science and Engineering, Soongsil University, [2]Department of Semiconductor Engineering, GIST

철 회

2026년 1월 29일(목), 09:00-10:45
Room E(5층, 에메랄드)

J. Nano-Science & Technology 분과

O33_[TE1-J] 공정·계면·재료공학 기반 나노전자

좌장: 김태욱 교수(전북대학교), 조준현 교수(전북대학교)

초청발표 **TE1-J-1** 09:00-09:30	**Topological van der Waals Contacts for 2D Materials** Soheil Ghods[1,2], Hochan Jang[1,2], Ji-Yun Moon[2,3,4], and Jae-Hyun Lee[1,2] [1]Department of Electrical and Computer Engineering, Sungkyunkwan University, [2]Center for Stacked van der Waals Semiconductors, Sungkyunkwan University, [3]Department of Mechanical Engineering and Materials Science, [4]Institute of Materials Science and Engineering, Washington University
TE1-J-2 09:30-09:45	**Study on the Effects of Formation Temperature of Alkanethiol Self-Assembled Monolayers on their Electrical Properties** Hyemin Lee[1], Haeri Kim[2], Donguk Kim[1], Jongwoo Nam[1], Minwoo Song[1], Hyun Sun Sung[2], Jaegeun Noh[2], and Takhee Lee[1] [1]Department of Physics and Astronomy, Seoul National University, [2]Department of Chemistry, Hanyang University
TE1-J-3 09:45-10:00	**Passivation of Indium Selenide: Suppressing Polymer-Induced Doping through Redox Activation** Jieun Jo[1], Chan Kwon[1], Hyeon Jung Park[1], Chaewon Lee[1], Haneul Kim[1], Taehoon Kim[1], Ga Hyun Cho[1], Seungho Bang[1], Dae Young Park[2], and Mun Seok Jeong[1] [1]Hanyang University, [2]Sungkyunkwan University
TE1-J-4 10:00-10:15	**Phase-Engineered Amorphous-Tellurium Trioxide: An Emerging p-Type Channel Material** Seungho Bang[1], Chaewon Lee[1], Deogkyu Choi[1], Dae Young Park[1], Dong Hyeon Kim[1], Dohyeon Lee[1], Dong-Joon Yi[1,2], Jungeun Song[3], Seok Joon Yun[4], Dong-Wook Kim[3], and Mun Seok Jeong[1] [1]Department of Physics, Hanyang University, [2]Department of Electronics Engineering, Hanyang University, [3]Department of Physics, Ewha Womans University, [4]Department of Semiconductor Physics and Engineering, University of Ulsan
TE1-J-5 10:15-10:30	**Uniform Sub-60 mV/dec Super-Steep Subthreshold Swing Achieved in Chip-Scale Graphene/IGZO Cold Source FET Array** Seyoung Oh[1,2], Jonghun Jeon[1], Jaeyoung Yoon[1], and Byungjin Cho[1,2] [1]Department of Advanced Materials Engineering, Chungbuk National University, [2]Department of Urban, Energy, and Environmental Engineering, Chungbuk National University
TE1-J-6 10:30-10:45	**Capacitance-Voltage Characterization as a Diagnostic Tool for Dielectric Selection in VCMA Devices** Ji-Hyeon Yun[1,2], Kyumin Sim[3], Yeon-Su Park[4], In-Kook Hwang[1], Sang Ho Lim[2], Byong-Guk Park[4], Hamin Park[3], and Seung-heon Chris Baek[1] [1]Center for Semiconductor Technology, KIST, [2]Department of Materials Science and Engineering, Korea University, [3]Department of Electronic Engineering, Kwangwoon University, [4]Department of Materials Science and Engineering, KAIST

2026년 1월 29일(목), 09:00-10:45
Room F(5층, 사파이어)

K. Memory (Design & Process Technology) 분과

O34_[TF1-K] Ferroelectric

좌장: 심원보 교수(서울과학기술대학교), 구민석 교수(서울시립대학교)

TF1-K-1 09:00-09:15	**Memory Window Expansion in $Hf_{0.5}Zr_{0.5}O_2$ MFS FeFETs Enabled by ZrO_2 Interlayer** Eunjin Kim and Jiyong Woo School of Electronic and Electrical Engineering, Kyungpook National University
TF1-K-2 09:15-09:30	**Domain-Engineered $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Tunnel Junction with Oxygen Vacancy Suppression for Enhanced Endurance** Hyojin Yang, Seongho Park, Minwoo Kim, Dae Hwan Kim, Sung-Jin Choi, and Yoon Jung Lee School of Electrical Engineering, Kookmin University
TF1-K-3 09:30-09:45	**AI 메모리 구현을 위한 고성능 강유전체 소자 기술 특허 출원 동향** 한상국, 정재훈, 김희태 지식재산청 반도체심사추진단
TF1-K-4 09:45-10:00	**Effect of Electrode Work-Function Asymmetry on Built-in Fields in Ferroelectric ALD-HZO Thin Films** Hoyoung Kim, Gwanghyeon Jang, Seongbin Lee, Hyeonhong Min, Yechan Kim, Soohyeok Park, Geonhwi Kim, Yejin Han, Han-Don Um, and Si Joon Kim Kangwon National University
TF1-K-5 10:00-10:15	**Dual-Gate HZO Ferroelectric Field-Effect Transistor with Gd-Doped HfO_2 Top-Gate Insulator** Jin Yeong Lee[1], KyungSoo Park[2], HyeonCheol Jeong[1], SangMyum Lim[1], TaeSuk Kim[2], GyuMin Hwang[1], YeonWoo Choi[1], Jihoon Choi[1], YoonSeok Lee[1], YeJun Park[1], Hanbyul Kim[3], Yongjoo Park[3], and Changhwan Choi[1,2] [1]Division of Semiconductor Engineering, Hanyang University, [2]Department of Materials Science and Engineering, Hanyang University, [3]SK Trichem Co., Ltd.
TF1-K-6 10:15-10:30	**HfLaO 박막을 이용한 하프니아 기반 FeFET의 Disturbance 특성 완화** 김승훈[1], 유찬미[2], 박영근[1], 정원묵[1], 이동규[2], 조병진[1,2] [1]한국과학기술원 전기 및 전자공학부, [2]한국과학기술원 반도체공학대학원
TF1-K-7 10:30-10:45	**Impact of Ferroelectric/Insulator Interface Traps on the Memory Characteristics of Metal-Ferroelectric-Insulator-Semiconductor FeFET** Seok-Hoon Jeong[1], Ha-Neul Lee[2], Sujong Kim[2], Eunchong Kim[1], Hwanjin Kim[2], Haesung Kim[3], Hyojin Yang[2], and Jong-Ho Bae[1] [1]Department of System Semiconductor Engineering, Yonsei University, [2]School of Electrical Engineering, Kookmin University, [3]Birck Nanotechnology Center, Purdue University

2026년 1월 29일(목), 09:00-10:45
Room G(5층, 루비 II)

C. Material Growth & Characterization 분과

O35_[TG1-C] Ferroelectricity and Complex Oxides

좌장: 서준민 교수(서울대학교), 엄기태 교수(가천대학교)

초청발표 **TG1-C-1** 09:00-09:30	**Optical Spectroscopic Characterization of High κ and Ferroelectric Oxides** Changhee Sohn Department of Physics, UNIST
TG1-C-2 09:30-09:45	**Kinetic Control of Cation Stoichiometry in Infinite-Layer Cuprate by Pulsed Laser Deposition** Jaewoo Lee[1,2], Jiwon Lee[1,2], Hyungmok Lee[1,2], and Woo Jin Kim[1,2] [1]Department of Materials Science and Engineering, Pusan National University, [2]Institute of Materials Technology, Pusan National University
TG1-C-3 09:45-10:00	**Epitaxial Stabilization of van der Waals-Layered α-MoO_3 Thin Films** Hyeondong Do[1,2], Donghoon Shin[1], and Woo Jin Kim[1,2] [1]Department of Materials Science and Engineering, Pusan National University, [2]Institute of Materials Technology, Pusan National University
TG1-C-4 10:00-10:15	**In-situ TEM Study on Structural and Defect Responses of $Hf1/2Zr1/2O_2$ under Heating and Biasing Conditions** Jeehun Jeong[1], Heechan Bang[2], Minchan Seong[1], Keeyong Lee[1], Chan-Ho Yang[2], and Sang Ho Oh[1] [1]Department of Energy Engineering, KENTECH, [2]Department of Physics, KAIST
초청발표 **TG1-C-5** 10:15-10:45	**Sub-Unit-Cell-Segmented Ferroelectricity in Brownmillerite Oxides by Phonon Decoupling** Si-Young Choi[1,2,3] [1]Department of Materials Science and Engineering, POSTECH, [2]Department of Semiconductor Engineering, POSTECH, [3]Center for Van der Waals Quantum Solids, IBS

2026년 1월 29일(목), 09:00-10:45
Room H(6층, 스페이드)

G. Device & Process Modeling, Simulation and Reliability 분과

O36_[TH1-G] Device & Process Modeling, Simulation and Reliability IV

좌장: 이재현 교수(부산대학교), 홍성민 교수(GIST)

초청발표 **TH1-G-1** 09:00-09:30	**Quantum Simulations for Advanced Logic Devices and Interconnects** Yeonghun Lee Department of Electronics Engineering, Incheon National University
TH1-G-2 09:30-09:45	**Component Based Quantification of Trap Formation in MOS Devices under Total Ionized Dose Stress** Jung Woo Moon[1,2], Jemin Kim[1], Kwanhun Lee[1], Byungjin Ma[1], and Youngbin Lee[1] [1]Reliability Technology Research Center, KETI, [2]Department of Chemical and Biomolecular Engineering, Yonsei University
TH1-G-3 09:45-10:00	**Temperature-Dependent Characterization and SPICE-Based Compact Modeling of a Dual-Gate Feedback Field-Effect Transistors** Jaewon-Lee and Min-Woo Kwon Department of Electronic Engineering, Seoul National University of Science & Technology
TH1-G-4 10:00-10:15	**Introduction to Hybrid ESD Model Using HSPICE and Verilog-A** Dongseok Han, Seungchan Yun, Minsu Choi, Bongsik Sihn, Inho Hwang, Gyeongsun Park, Suk Yun, and Ilsup Jin Future Technology Group, SK Keyfoundry Co., Ltd
TH1-G-5 10:15-10:30	**Charge Pumping-Based Characterization of Interface Trap Density and Reliability of FeFETs for Cryogenic Operation** Sangmyun Lim[1], Kyungsoo Park[2], Sangkuk Han[2], HyeonCheol Jeong[1], Jihoon Choi[1], Taesuk Kim[2], Haesoo Jang[1], Jaewon Chung[1], Wonjae Choi[1], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University
TH1-G-6 10:30-10:45	**Reliability Comparison of BJTs with Different Emitter Areas under Electrical Stress Conditions** Ju-Han Lee, Ju-Yong Shin, Yu-Bin Kim, and Hi-Deok Lee Department of Electronics Engineering, Chungnam National University

2026년 1월 29일(목), 09:00-10:45
Room I(6층, 하트)

F. Silicon and Group-IV Devices and Integration Technology 분과

O37_[TI1-F] Ferroelectric Device Technology

좌장: 이병훈 교수(POSTECH), 황현준 교수(목포대학교)

TI1-F-1 09:00-09:15	**Fatigue and Recovery Mechanism of $HfZrO_2$/Ge MF(I)S Capacitors under Low Operating Voltage** Jai-Youn Jeong[1,2], Kyul Ko[1], Changhwan Shin[2], and Jae-Hoon Han[1] [1]Center for Quantum Technology, KIST, [2]Device and Circuit Laboratory, Korea University
TI1-F-2 09:15-09:30	**Oxygen Vacancy Engineering of ITO Interfacial Layer for Enhanced Reliability in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Capacitors** Haevin Choi and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University
TI1-F-3 09:30-09:45	**Improved Ferroelectricity in W/$Hf_{0.5}Zr_{0.5}O_2$/W Capacitor With WOx Interlayer** Juneyup Cho and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University
TI1-F-4 09:45-10:00	**Capacitance Wake up in Morphotropic Phase Boundary Enabled by Bilayer $Hf_xZr_{1-x}O_2$ Capacitors** Junseok Kim and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University
TI1-F-5 10:00-10:15	**The Strategy to Enhance "On" State Current of Ferroelectric Tunnel Junction Satisfying Self-Rectifying Property** Hui Seong Shin, Sehee Kim, and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University
TI1-F-6 10:15-10:30	**Hf-Free Ferroelectric Capacitor with ZrO_2/Oxide Semiconductor for Low-Power Non-Volatile Operation** Changwoo Han[1], Hyeonjung Park[2], Inhyeok Choi[3], and Changhwan Shin[1] [1]School of Electrical Engineering, College of Engineering, Korea University, [2]Department of Electrical and Computer Engineering, Sungkyunkwan University, [3]Department of Physics, College of Science, Korea University
TI1-F-7 10:30-10:45	**The Role of IGZO Interlayer as an Oxygen Reservoir Layer for Enhanced Ferroelectric Capacitor Endurance** Donghyeon Kim and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University

2026년 1월 29일(목), 09:00-10:45
Room J(6층, 다이아몬드)

I. MEMS & Sensors Systems 분과

O38_[TJ1-I] MEMS and Sensor System II

좌장: 상민규 교수(가천대학교), 유호천 교수(한양대학교)

TJ1-I-1 09:00-09:15	**Wireless Multi-Sensing System for Real-Time Battery Safety Management** Junghoon Lee[1], Hyejun Kim[1], Seongu Kim[1], Yeonjae Yang[1], Jinsu Park[1], Sangkyu Lee[2], and Jeonghyun Kim[1] [1]Department of Electronic Convergence Engineering, Kwangwoon University, [2]Department of Energy Science & Engineering, Kunsan National University
TJ1-I-2 09:15-09:30	**Development of a Ferroelectric Ga-HfO_2 Thin Film via Co-Sputtering for Vibration and Temperature Sensor** Minsoo Kim[1], Junmo Kim[1], Minje Lee[1], Donghyeon Bae[1], and Hyeongtak Seo[1,2] [1]Department of Energy Systems Research, Ajou University, [2]Department of Materials Science and Engineering, Ajou University
TJ1-I-3 09:30-09:45	**Solution-Processable and Photo-Patternable Electronic Materials for Transient Electronics** Sungkeun Han[1] and Suk-Won Hwang[1,2,3] [1]KU-KIST Graduate School of Converging Science and Technology, Korea University, [2]Center for Biomaterials, Biomedical Research Institute, KIST, [3]Department of Integrative Energy Engineering, Korea University
TJ1-I-4 09:45-10:00	**Magneto-Encephaloscope: A Minimal-Invasive and Magnetically Controllable Neural Interface** Jeongmin Yoo[1], Sang Hoon Park[2], Ji Won Lee[2], Gyuri Shin[1], Yeonhee Heo[1], Ki Jun Yu[2], and Yoonseok Park[1] [1]Department of Materials Science and Engineering, Kyung Hee University, [2]School of Electrical and Electronic Engineering, Yonsei University
TJ1-I-5 10:00-10:15	**Wearable Ring Sensor for Enhanced Accuracy and Comfort in Blood Pressure Monitoring** Seongu Kim, Lurong Yang, Hyejun Kim, Junghoon Lee, Yeonjae Yang, Jinsu Park, and Jeonghyun Kim Department of Electronic Convergence Engineering, Kwangwoon University
초청발표 **TJ1-I-6** 10:15-10:45	**Acoustic Impedance Mismatching for Ultrasound-driven Triboelectric Generator** Hong-Joon Yoon[1,2] [1]Department of Electronic Engineering, Gachon University, [2]Department of Semiconductor Engineering, Gachon University

2026년 1월 29일(목), 10:55-12:40
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O39_[TC2-D] Ferroelectrics II

좌장: 이홍섭 교수(경희대학교), 유찬영 교수(홍익대학교)

TC2-D-1 10:55-11:10	**Enhancement of Polarization Characteristics in HZO-Based FeCAP Using a Dual Insertion Layer Structure** Dongchan Seo[1], Taehyung Kim[1], Kiwon Yoon[2], and Jinsub Park[1,2] [1]Department of Electronic Engineering, Hanyang University, [2]Department of AI Semiconductor Engineering, Hanyang University
TC2-D-2 11:10-11:25	**Enhanced Ferroelectricity in $Hf_{0.5}Zr_{0.5}O_2$ Thin Films via Ar Plasma Surface Treatment** Jeonggwang Lee[1], Jaewook Lee[1], Hyun Woo Jeong[1], Hyojun Choi[1], Young Yong Kim[2], and Min Hyuk Park[1] [1]Department of Materials Science and Engineering, Seoul National University, [2]Pohang Accelerator Laboratory, POSTECH
TC2-D-3 11:25-11:40	**Nanolaminate-Driven Ferroelectric Enhancement in Ultrathin $(Hf,Zr)O_2$ with Quantitative Strain Analysis** Jaewook Lee, Hyun Woo Jeong, Yong Hyeon Cho, and Min Hyuk Park Department of Materials Science and Engineering, Seoul National University
TC2-D-4 11:40-11:55	**Lowering Effective Dielectric Constant of Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Film with an Ultra-Thin Al_2O_3 Intermediate Layer** Jinyoung Park[1], Hyunjae Park[2], Hyunmin Kwun[2], Eunseok Hyun[2], Jaehyeong Jo[2], Jiwan Kim[2], Wonho Song[3], Junhyung Kim[4], and Kibog Park[1,5] [1]Semiconductor R&D Center, Samsung Electronics Co., Ltd.,[2]Department of Physics, UNIST, [3]LG Display Co., Ltd., [4]ETRI, [5]Department of Electrical Engineering, UNIST
TC2-D-5 11:55-12:10	**Role of Nitrogen Content in Determining the Reliability of Symmetric MoN_x-Based Ferroelectric Capacitors** Hyojun Choi, Ju Yong Park, Jaewook Lee, Hyun Woo Jeong, Dong In Han, Sun Young Lee, Kun Yang, and Min Hyuk Park Department of Materials Science and Engineering, Seoul National University
TC2-D-6 12:10-12:25	**In Situ Analysis of Wake-Up Induced Phase Transition and In-Plane Strain Modulation in $Hf_{0.5}Zr_{0.5}O_2$ Thin Films via Grazing Incidence Synchrotron X-Ray Diffraction** Hyun Woo Jeong[1], Younghwan Lee[2], and Min Hyuk Park[1] [1]Department of Materials Science and Engineering, Seoul National University, [2]School of Materials Science and Engineering, Chonnam National University
TC2-D-7 12:25-12:40	**잔류 분극 구동 기반 IGZO FeTFT의 계면 트랩 정량화 연구** 조성조, 박소영, 고운산, 홍혜리, 이가원 충남대학교 전자공학과

2026년 1월 29일(목), 10:55-12:40
Room D(5층, 컨벤션홀 L)

E. Compound Semiconductors 분과

O40_[TD3-E] Optical and Other Device Technologies

좌장: 허준석 교수(아주대학교), 황완식 교수(한국항공대학교)

TD3-E-1 10:55-11:10	**InGaAs/InP Phototransistor Heterogeneously Integrated on Si Photonics Platform** Kyunghwan Kim[1], Yuna Lee[1], Sanghyeon Kim[2,3], and Jae-Hoon Han[1] [1]Center for Quantum Technology, KIST, [2]School of Electrical Engineering, KAIST, [3]Graduate School of Semiconductor Technology, KAIST
TD3-E-2 11:10-11:25	**III-V/Ins./Si Waveguide-integrated High-Speed Mach-Zehnder Optical Modulator for Co-packaged Optics** Donggil Kang[1], Shin Hyung Lee[1], Jae-Hoon Han[2], Jongmin Kim[3], Seok-Geun Ahn[4], Minhyuk Jung[4], Hyun-Chul Jung[4], and SangHyeon Kim[1] [1]School of Electrical Engineering, KAIST, [2]KIST, [3]KANC, [4]Samsung Electronics Co., Ltd.
TD3-E-3 11:25-11:40	**Monolithic Growth of High-Quality InSb on On-Axis (001) Silicon for Mid-Wavelength Infrared Photodetector Applications** Kenneth Duque[1,2], Tsimafei Laryn[1,2], Seungwan Woo[1,3,4], Eunkyo Ju[1,5], Eungbeom Yeon[1,5], Yeonhwa Kim[1,5], In-Hwan Lee[5], Won Jun Choi[1], and Daehwan Jung[1,2] [1]Center for Quantum Technology, KIST, [2]Division of Nanoscience and Technology, KIST School at University of Science and Technology, [3]Department of Materials Science and Engineering, Seoul National University, [4]Research Institute of Advanced Materials, Seoul National University, [5]Department of Materials Science and Engineering, Korea University
TD3-E-4 11:40-11:55	**Monolithically Integrated InGaAs/InAsSb Ultra-Broadband Infrared Detector Covering 0.8 – 5.5 Micron Wavelengths** Seungwan Woo[1,2], Eungbeom Yeon[1], Ho Won Jang[2], Daehwan Jung[1], and Won Jun Choi[1] [1]Center for Quantum Technology, KIST, [2]Department of Materials Science and Engineering, Seoul National University
TD3-E-5 11:55-12:10	**중적외선 검출을 위한 유연 기판 위 T2SL 광검출기 Array 제작** 한재훈 한국과학기술연구원 양자기술연구단
TD3-E-6 12:10-12:25	**Improved Specific Contact Resistivity in Amorphous IGZO via Sub-Nanometer SiO_2 Interlayer Engineering** So Young Lim[1], Taewon Hwang[1], Sangwoo Lee[2], and Jin-Seong Park[1] [1]Division of Materials Science and Engineering, Hanyang University, [2]Tokyo Electron Korea Ltd.
TD3-E-7 12:25-12:40	**Al-Doped NiO/β-Ga_2O_3 P-N Heterojunction Diodes for Enhanced Electrical and Thermal Characteristics** Ho Jung Jeon[1,2,3] and You Seung Rim[1,2,3] [1]Department of Semiconductor Systems Engineering, Sejong University, [2]Department of Convergence Engineering for Intelligent Drone, Sejong University, [3]Institute of Semiconductor and System IC, Sejong University

2026년 1월 29일(목), 10:55-12:40
Room E(5층, 에메랄드)

J. Nano-Science & Technology 분과

O41_[TE2-J] 광전자·포토닉 디바이스 및 센서

좌장: 이철호 교수(서울대학교), 이재현 교수(성균관대학교)

초청발표 **TE2-J-1** 10:55-11:25	**Interfacial Engineering in Layered Magnetic Semiconductor CrSBr** Junhyeon Jo Division of Advanced Materials Engineering, Jeonbuk National University
TE2-J-2 11:25-11:40	**Metal-Silicon-Metal Hot-Carrier Avalanche Photodetector for High-Responsivity SWIR Detection** Ji-Hwan Son[1,2], Eui-Hyoun Ryu[1], Sunghyun Hwang[1], Nayeon Kim[1], Nayoung Kim[1], Myung-Jae Lee[3], Jae-Hoon Han[1], and In-Ho Lee[11]Center for Quantum Technology, KIST, [2]Department of Micro/Nano Systems, Korea University, [3]Department of Electrical and Electronic Engineering, Yonsei University
TE2-J-3 11:40-11:55	**Focused-Beam-Induced Asymmetric Guided-Mode Resonance for Compact Optical Sensors** Yeong Hwan Ko Kongju National University
TE2-J-4 11:55-12:10	**A Transfer-Free Solution-Processed MoS_2 Based mmWave Switches with f_{co} ~ 94 THz for Radiofrequency Circuit Application** Changwoo Pyo[1], Sungmoon Park[1], and Myungsoo Kim[1,2] [1]Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [2]Department of Electrical Engineering, UNIST
TE2-J-5 12:10-12:25	**Enabling Frequency-Agile Reconfigurable X-Band Filters with VO_x-Based Non-Volatile RF Switches** Dabin Seo[1], Dahyeon Kim[2], and Myungsoo Kim[1,2] [1]Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [2]Department of Electrical and Computer Engineering, UNIST
TE2-J-6 12:25-12:40	**A Flexible and Thermally Stable Polymer-Based Analogue Switch for Millimeter-Wave Systems** Sungmoon Park[1], Changwoo Pyo[1], Ji Ho Yu[2], Min Ju Kim[2], and Myungsoo Kim[1] [1]Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [2]Department of Foundry Engineering, Dankook University

2026년 1월 29일(목), 10:55-12:55
Room F(5층, 사파이어)

K. Memory (Design & Process Technology) 분과

O42_[TF2-K] DRAM

좌장: 정두석 교수(한양대학교), 전종욱 교수(성균관대학교)

초청발표 **TF2-K-1** 10:55-11:25	**Scaling Challenges and Emerging Solutions for DRAM Cell Transistors Beyond Sub 10 nm Node** Seol-Min Yi, Seon Soon Kim, Young-man Cho, and Seon Yong Cha R&D, SK hynix Inc.
TF2-K-2 11:25-11:40	**Surrounding Poly-Si Capacitor-Implemented 2T DRAM Cell for Retention Improvement and Coupling Effect Suppression** Seonghwan Kong and Wonbo Shim Department of Electrical and Information Engineering, Seoul National University of Science & Technology
TF2-K-3 11:40-11:55	**Optimizing Novel 3D-Stackable 2T0C DRAM Cell Design through TCAD Simulation and Its Experimental Verification** Yongwoo Ryu[2], Gyuheon Bae[2], Youngjoon Lee[3], Dae Hwan Kang[1,2], and Changwook Jeong[3] [1]Department of Semiconductor Engineering, POSTECH, [2]Graduate School of Semiconductor Technology, POSTECH, [3]Graduate School of Semiconductor Materials and Devices Engineering, UNIST
TF2-K-4 11:55-12:10	**A Split-Gate 2T0C Gain Cell Suppressing Cell-Level and Array-Level Issues** Jeong-Min Lee[1], Seung-Yoon Lee[2], Seong-Jun Byun[1], and Joon-Kyu Han[1] [1]Department of Materials Science and Engineering, Seoul National University, [2]Department of Electronic Engineering, Sogang University
TF2-K-5 12:10-12:25	**Investigation of Low-Frequency Noise Characteristics in Charge-Trap-Based DRAM Devices** Hyokyung Kim[1], Hyeongyu Kim[1], Yoojin Seol[1], Jeongmin Son[1], and Kihyun Kim[1,2] [1]Department of Electronics and Information Engineering, Jeonbuk National University, [2]Division of Electronic Engineering, Jeonbuk National University
TF2-K-6 12:25-12:40	**TCAD-SPICE 혼합모드 기반 소자-특성 반영 DRAM 센스앰프 기본 회로 동작 특성 평가** 박제원[1], 김건[1], 김동영[1], 김수연[1], 김신욱[1], 강륜[1], 김소원[1], 임채혁[1], 윤정현[1], 서현아[1], 이혜린[1], 이주원[1], 최우진[2], 김어진[2], 정민우[2], 이명진[2] [1]전남대학교 지능전자컴퓨터공학과, [2]전남대학교 전자컴퓨터공학부
TF2-K-7 12:40-12:55	**Memristor-Based Artificial Sensory Nervous System for Neuro-Inspired Robotics** See-On Park[1], Hakcheon Jeong[2], Seokho Seo[2], Youna Kwon[3], Jongwon Lee[4], and Shinhyun Choi[1,2] [1]Information and Electronics Research Institute, KAIST, [2]School of Electrical Engineering, KAIST, [3]Nano Convergence Technology Division, NNFC, [4]Department of Semiconductor Convergence, Chungnam National University

2026년 1월 29일(목), 10:55-12:40
Room G(5층, 루비 II)

C. Material Growth & Characterization 분과

O43_[TG2-C] BEOL & Semiconductor Integration Technologies

좌장: 최시영 교수(POSTECH), 송승욱 교수(성균관대학교)

초청발표 **TG2-C-1** 10:55-11:25	**BEOL-Compatible Monolithic Integration of Property-Tunable Complex Oxide Single Crystals on Si for Advancing the More-than-Moore Paradigm** Seung-Hyub Baek Electronic and Hybrid Materials Research Center, KIST
TG2-C-2 11:25-11:40	**Additive Manufacturing and Densification of SiC-Based Components for Semiconductor Processing Equipment** Youngsuk Jung, Ji-Won Oh, and Shinhu Cho MADDE Inc.
TG2-C-3 11:40-11:55	**Record-low Threading Dislocation Density of GaSb on Si Buffer Template via Optimized Multiple Defect Filter Layers** Eungbeom Yeon[1,2], Seungwan Woo[1], In-Hwan Lee[2], Daehwan Jung[1], and Won Jun Choi[1] [1]Center for Quantum Technology, KIST, [2]Department of Materials Science and Engineering, Korea University
TG2-C-4 11:55-12:10	**Thermal Atomic Layer Deposition of TiN Using Metal Organic Precursors with N_2H_4 Reactant** 최윤서, 박혜원, 이한보람 인천대학교 신소재공학과
TG2-C-5 12:10-12:25	**Tunable Dielectric Trap Engineering of SiN_x for Operating Voltage Modulation in Charge Trap Flash Memory** Hanyeol Ahn[1], Minseon Gu[1], Hyun Don Kim[1,2], Seungchul Choi[1], Hyun Su Park[1], Sangwoo Nam[1,2], Kyu-Myung Lee[3], Yongsup Park[3], Jinwoo Byun[5], Gukhyon Yon[5], E.J. Choi[1], Young Jun Chang[1,4], and Moonsup Han[1] [1]Department of Physics, University of Seoul, [2]Department of Smart Cities, University of Seoul, [3]Department of Physics, Kyung Hee University, [4]Department of Intelligent Semiconductor, University of Seoul, [5]Advanced Process Development Team, Semiconductor R&D Center, Samsung Electronics Co., Ltd.
TG2-C-6 12:25-12:40	**Epitaxial Growth of 775 nm $Al_{0.1}Ga_{0.9}As$ and $In_{0.1}Al_{0.2}Ga_{0.7}As$ Quantum Well Laser Diodes for Quantum Photonic Applications** Tsimafei Laryn[1,2], Yeonhwa Kim[1,3], Kenneth Duque[1,2], Won Jun Choi[1], and Daehwan Jung[1,2] [1]Center for Quantum Technology, KIST, [2]Division of Nanoscience and Technology, KIST School at University of Science and Technology, [3]Department of Materials Science and Engineering, Korea University

2026년 1월 29일(목), 10:55-12:40
Room H(6층, 스페이드)

T. AI 분과

O44_[TH2-T] Artificial Intelligence I

좌장: 김병수 센터장(KETI), 이재학 팀장(KETI)

초청발표 **TH2-T-1** 10:55-11:25	**Development Direction of Server PIM Platform for Large Language Models** Kyu Hyun Choi and Jae Hyung Ko SoC Platform Research Center, KETI
TH2-T-2 11:25-11:40	**Real-Time Prediction of 3D-to-2D Surface Transition during GaN Epitaxial Growth Using an In Situ RHEED-Based Transformer Model** Jun Suk Chang, Hyeong Yeon Lee, and Hong Kyun Noh AI Manufacturing Division, IVWorks Co., Ltd.
TH2-T-3 11:40-11:55	**Timestep-wise Token Merging for Efficient Spiking Transformer** Minyeong An and Jongsun Park Department of Electrical Engineering, Korea University
TH2-T-4 11:55-12:10	**Artificial Neural Logic Operators for Energy-Efficient Dendritic Computing** Unhyeon Kang[1,2], Seungmin Oh[1,3], Jingyeong Hwang[1,2], Jiin Bang[1,4], Kyungmin Lee[1,5], Hakseung Rhee[1,6], Younghyun Lee[1], Jooyoung Bae[1], and Suyoun Lee[1] [1]Center for Semiconductor Technology, KIST, [2]Department of Materials Science and Engineering, Seoul National University, [3]Department of Physics and Astronomy, Seoul National University, [4]Division of Nanoscience and Technology, University of Science and Technology, [5]School of Electrical Engineering, Korea University, [6]Department of Materials Science and Engineering, KAIST
TH2-T-5 12:10-12:25	**신경망회로를 활용한 PID 기반 피드백 제어를 위한 시스템 온 칩 구성** 유동우[1], 백돈규[2] [1]충북대학교 반도체공학전공, [2]충북대학교 반도체공학부
TH2-T-6 12:25-12:40	**DeepSCF: Physics-Inspired Neural Networks for Efficient Self-Consistent Charge Density Prediction** Minsu Jeong, Ryong-Gyu Lee, and Yong-Hoon Kim School of Electrical Engineering, KAIST

2026년 1월 29일(목), 10:55-12:40
Room I(6층, 하트)

Q. Metrology, Inspection, Analysis, and Yield Enhancement 분과

O45_[TI2-Q] Metrology, Inspection, Analysis, and Yield Enhancement I

좌장: 제갈원 박사(한국표준과학연구원), 손영훈 마스터(삼성전자)

초청발표 **TI2-Q-1** 10:55-11:25	**AI-Enhanced Pulsed Thermography for Surface Micro-Crack Inspection in Epoxy Molding Compounds of Semiconductor Packages** Jinsung Rho Department of Mechanical Engineering, Hanbat National University
초청발표 **TI2-Q-2** 11:25-11:55	**초고속 레이저 기반 화학기상증착을 이용한 3차원 유리 구조 표면 전도성 회로 형성 기술** 한승회, 허준석, 위찬웅 전남대학교 기계공학과
TI2-Q-3 11:55-12:10	**이중모드 열반사 현미경을 이용한 마이크로 전자소자의 정상 및 과도열 특성 분석** 정찬배, 김동욱, 정문경, 김동목, 장기수 한국기초과학지원연구원 연구장비개발부
TI2-Q-4 12:10-12:25	**열특성 기반 첨단반도체 패키지용 TGV 비파괴 고장분석 기술 제안** 마병진, 백주희, 이영빈, 최성순, 이규석, 김제민 한국전자기술연구원
TI2-Q-5 12:25-12:40	**Tip-Enhanced Nano-Spectroscopy and Imaging for Applications in Semiconductor Metrology and Inspection** Kyoung-Duck Park[1,2] [1]Department of Physics, POSTECH, [2]Department of Semiconductor Engineering, POSTECH

2026년 1월 29일(목), 10:55-12:40
Room J(6층, 다이아몬드)

H. Display and Imaging Technologies 분과

O46_[TJ2-H] Semiconductor Photonics for Displays and Imagers

좌장: 정예환 교수(한양대학교), 노정균 교수(부산대학교)

초청발표 **TJ2-H-1** 10:55-11:25	**Next-generation III-V Semiconductor Infrared Photodetectors for Thermal Imaging Sensors** Daehwan Jung[1,2], Seungwan Woo[1], Kenneth Duque[1], Tsimafei Laryn[1,2], Eungbeom Yeon[1], Yeonhwa Kim[1], and Won Jun Choi[1] [1]Center for Quantum Technology, KIST, [2]Division of Nanoscience and Technology, KIST School, University of Science and Technology
초청발표 **TJ2-H-2** 11:25-11:55	**Photonic-Integrated Circuits and On-Chip Light Sources for Scalable Quantum Computing Technologies** 남동욱[1,2] [1]한국과학기술원 기계공학과, [2]한국과학기술원 양자대학원
TJ2-H-3 11:55-12:10	**Analyzing Dark Count Rate and Photon Detection Probability Characteristics of Single Photon Avalanche Diode without Hydrogen Annealing Process** 김상환, 정주환, 이한규, 유현, 윤찬수, 이경재, 하만륜, 이상기 Technology CIS Process Development Team, DB HiTek
TJ2-H-4 12:10-12:25	**A 10μm-Pitch Stand-Alone SPAD with 30.3% PDE at 940nm, Utilizing a Dual Epitaxial Growth Process and Full-BDTI with 2x2 Microlens Integration** Juhwan Jung, Sang Hwan Kim, Chansoo Yoon, Hyun Yoo, Gyeong Jae Lee, Man Lyun Ha, and Sang Gi Lee CIS Process Development Team, DB HiTek
TJ2-H-5 12:25-12:40	**Full Well Capacity Modeling of Vertical Pinned Photodiode with Realistic Photodiode Doping** 박지원[1], 이지원[1,2] [1]포항공과대학교 반도체대학원, [2]포항공과대학교 반도체공학과

2026년 1월 29일(목), 14:00-15:45
Room A(4층, 그랜드볼룸 I+II)

D. Thin Film Process Technology 분과

O47_[TA3-D] Emerging Devices II

좌장: 문태환 교수(아주대학교), 권대선 교수(숙명여자대학교)

TA3-D-1 14:00-14:15	**Atomic Layer Deposition of $Ge_XSe_YTe_Z$ Thin Films for Selector-only Memory** Hyun Wook Kim, Ju Hwan Park, Se Hwan Jeon, Tae Jun Yang, Yoon Jae Hong, Dong Hyun Kim, and Byung Joon Choi Department of Materials Science and Engineering, Seoul National University of Science & Technology
TA3-D-2 14:15-14:30	**Study on the Atomic-Layer-Deposited In-Te Films for Vertical Selector Only Memory Applications** Myeong Hwan You[2], Beom Joo Kim[2,3], and Dae Hwan Kang[1,2] [1]Department of Semiconductor Engineering, POSTECH, [2]Graduate School of Semiconductor Technology, POSTECH, [3]Department of Materials Science and Engineering, Chonnam National University
TA3-D-3 14:30-14:45	**Ultrathin Monatomic Antimony Films by Sacrificial Atomic Layer Deposition for Phase Change Memory** Sangmin Jeon[1,2], Gwangsik Jeon[1,2], Seunghwan Lee[1,2], Jeong Woo Jeon[1,2], Wonho Choi[1,2], Byongwoo Park[1,2], Sungjin Kim[1,2], Junwoo Park[1,2], Chanyoung Yoo[3], Hyejin Jang[1,2], and Cheol Seong Hwang[1,2] [1]Department of Materials Science and Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University, [3]Department of Materials Science and Engineering, Hongik University
TA3-D-4 14:45-15:00	**Atomic Layer Deposition of Sb_2Te_3/MnTe Superlattice Film for Vertical Phase Change Memory** Gwangsik Jeon[1,2], Wonho Choi[1,2], Byongwoo Park[1,2], Sangmin Jeon[1,2], Sungjin Kim[1,2], Junwoo Park[1,2], Chanyoung Yoo[3], and Cheol Seong Hwang[1,2] [1]Department of Materials Science and Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University, [3]Department of Materials Science and Engineering, Hongik University
TA3-D-5 15:00-15:15	**Multilayer Bi-GeSeTe SOM for Window-Margin Enlargement and Array-Level Reproducibility** Jae Jun Lee, Eun Taek Yu, Geon Woo Cheon, and Min Kyu Yang Artificial Intelligence Semiconductor Process Lab, Sahmyook University
TA3-D-6 15:15-15:30	**Enhanced Read Margin and Multilevel Switching Characteristics in W/GeAsSeTe/W Selector-Only Memory via Bi Doping** Min Kyung Lee[1], Ji Soo Han[2], Dong Hyun Lee[2], Se Eun Jeong[2], Hee Sang Park[2], Changhwan Shin[1], and Min Kyu Yang[2] [1]School of Electrical Engineering, Korea University, [2]Artificial Intelligence Semiconductor Process Lab, Sahmyook University
TA3-D-7 15:30-15:45	**Sn-Doped GSST Selector-Only Memory for Robust BNN Inference** Hyun Kyu Seo[1,2], Na Young Kim[1], Ji Won Song[1], Jae-Seung Jeong[1], Min Hyuk Park[2], and Min Kyu Yang[1] [1]Artificial Intelligence Semiconductor Process Lab, Sahmyook University, [2]Department of Materials Science and Engineering, Seoul National University

2026년 1월 29일(목), 14:00-15:45
Room B(4층, 그랜드볼룸 III)

B. Patterning (Lithography & Etch Technology) 분과

O48_[TB2-B] Patterning and Etch Materials

좌장: 김창구 교수(아주대학교), 채희엽 교수(성균관대학교)

초청발표 **TB2-B-1** 14:00-14:30	**Innovation of Patterning Materials in Semiconductor Technology** Seongjun Park Department of System Semiconductor Engineering, College of Engineering, Yonsei University
TB2-B-2 14:30-14:45	**Effect of H_2O Addition on Fluorocarbon Layer Formation on SiO_2 and Si_3N_4 Films in C_4F_8 Plasmas** Haegeon Jung[1,2], Hakseung Lee[1,2], Daeun Hong[3], Kangwoo Lee[3], Minsung Jeon[4], and Heeyeop Chae[1,4] [1]Department of Semiconductor and Display Engineering, Sungkyunkwan University, [2]Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd., [3]School of Chemical Engineering, Sungkyunkwan University, [4]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
TB2-B-3 14:45-15:00	**정전척(Electrostatic Chuck)의 주파수 응답 특성과 반도체 식각 공정(Etch Process)의 영향성 연구** 오병욱, 송완수, 강창진, 이윤영 PSK㈜ 연구개발본부
TB2-B-4 15:00-15:15	**Metal Seasoning 및 OES 장기 모니터링을 통한 Plasma Etch 설비의 Aging 방법론** 유하늘[1], 임재용[1], 김수정[1], 이현기[1], 최두원[2], 서봉임[2], 이원석[2], 조성민[1], 금의석[1] [1]삼성전자 Digital Twin센터, [2]삼성전자 메모리제조기술센터
TB2-B-5 15:15-15:30	**Coupling between Diffusion and Surface Reaction in Atomic Layer Etching** Sangheon Lee Department of Chemical Engineering and Materials Science, Ewha Womans University
TB2-B-6 15:30-15:45	**$CF_4/Ar/O_2$ 분위기에서 높은 물리화학적 플라즈마 식각 저항성을 지닌 고엔트로피 산화물 세라믹** 마호진 경기대학교 신소재화학공학부 신소재공학전공

2026년 1월 29일(목), 14:00-15:45
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O49_[TC3-D] Thin Film Transistors I

좌장: 안지훈 교수(한양대학교), 최병준 교수(서울과학기술대학교)

TC3-D-1 14:00-14:15	**Impact of Deposition and Annealing Conditions on Reliability and Performance in BEOL-Compatible Monolithic 3D IGZO Transistors** Min-Joe Lee, Ji-Won Kang, and Sung-Min Yoon Kyung Hee University
TC3-D-2 14:15-14:30	**Investigation for W Contact on IGZO TFT via Deuterium Annealing for Suppressed Oxygen Diffusion** Woosub Byun[1], Tae-Hyun Kil[2], Hwanyeol Park[3], Junyoung Park[2,4], and Dae-Myeong Geum[1] [1]Department of Electrical and Computer Engineering, Inha University, [2]ParkLab Semiconductor Inc, [3]Department of Display Materials Engineering, Soonchunhyang University, [4]School of Electronics Engineering, Chungbuk National University
TC3-D-3 14:30-14:45	**Source/Drain Overlap Length Dependence on the Electrical Performance of a-IGZO TFTs with Ti-Electrodes** Junhui Park[1], Jaewook Yoo[1], Hongseung Lee[1], Seongbin Lim[1], Minah Park[1], Seohyeon Park[1], Sojin Jung[1], Sieun Lee[1], Donghyeon Lee[1], Soohyun Lim[1], Dongsun Shin[1], Kiyoung Lee[3], Sung Hun Jin[2], and Hagyoul Bae[1] [1]Jeonbuk National University, [2]Kyung Hee University, [3]Hongik University
TC3-D-4 14:45-15:00	**Correlation of Hydrogen and Oxygen Composition with Transition Region Voltage in Oxide TFTs** Junseok Lee[1], Soohong Eo[1], Jae Woo Lee[1], Changwook Kim[1], Sung-Jin Choi[1], Yoon Jung Lee[1], Jaeman Jang[2], Ju Heyuck Baeck[2], Byung Du Ahn[2], Jong Uk Bae[2], Soo Young Yoon[2], and Dae Hwan Kim[1] [1]School of Electrical Engineering, Kookmin University, [2]R&D Center, LG Display Co., Ltd.
TC3-D-5 15:00-15:15	**Revealing Local Heterogeneity in a-IGZO through 4D-STEM and EELS** Daeyeong Kim, Keeyong Lee, Jinho Byun, Geun Ho Gu, and Sang Ho Oh Department of Energy Engineering, KENTECH
TC3-D-6 15:15-15:30	**Controllable Subthreshold Swing in Driving Oxide TFTs Enabled by Sn Delta Layer** Jae Young Lee[1] and Jae Kyeong Jeong[2] [1]Department of Artificial Intelligence Semiconductor Engineering, Hanyang University, [2]Department of Electronic Engineering, Hanyang University
TC3-D-7 15:30-15:45	**Electrical Pulse Signal for Enhancement of Electrical Performances in In_2O_3 TFTs** Dongsun Shin[1], Jaewook Yoo[1], Hongseung Lee[1], Sojin Jung[1], Seongbin Lim[1], Seohyeon Park[1], Minah Park[1], Donghyeon Lee[1], Soohyun Lim[1], Sieun Lee[1], Junhui Park[1], Kiyoung Lee[2], and Hagyoul Bae[1] [1]Jeonbuk National University, [2]Hongik University

2026년 1월 29일(목), 14:00-15:45
Room D(5층, 컨벤션홀 L)

K. Memory (Design & Process Technology) 분과

O50_[TD3-K] Adv. Memory & Ferroelectric

좌장: 강대웅 교수(서울대학교), 조우영 교수(KAIST)

초청발표 **TD3-K-1** 14:00-14:30	**Next Generation NAND Technology** Wanki Kim Semiconductor Research and Development, Samsung Electronics Co., Ltd.
TD3-K-2 14:30-14:45	**Ferroelectric Memcapacitor Crossbar Array with NAND Flash Structure for In-Memory Computing** Hwiho Hwang[1,2], Sangwook Youn[1,2], and Hyungjin Kim[1,2] [1]Division of Materials Science and Engineering, [2]Hanyang University, Department of Semiconductor Engineering, Hanyang University
TD3-K-3 14:45-15:00	**BEOL-Compatible FeTFTs With Ultra-Thin 3 nm HZO / 3 nm Oxide Semiconductor Stack (Physical) Enabling Low-Voltage Operation for Next-Generation Non-Volatile Memory** Kyungsoo Park[1], Minhyuk Kim[1], Duho Kim[1], Jihoon Choi[2], Yeonwoo Choi[2], Jin Yeong Lee[2], Taesuk Kim[1], Hyeoncheol Jeong[2], and Changhwan Choi[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University
TD3-K-4 15:00-15:15	**후면 강유전체 기반 이중 게이트 소자를 이용한 Read Disturbance 현상을 억제할 수 있는 AND-type 어레이 구조** 정재중[1], 박영근[1], 김예은[2], 김영권[3], 정원묵[4], 유찬미[4], 김승훈[1], 김영준[4], 강대현[1], 장병철[3], 박종경[2], 조병진[1,4] [1]한국과학기술원 전기및전자공학부, [2]서울과학기술대학교 지능형반도체공학과, [3]경북대학교 전자전기공학부, [4]한국과학기술원 반도체공학대학원
TD3-K-5 15:15-15:30	**Towards Artificial Intelligence Hardware with Monolithic 3D Integrated Ferroelectric Transistors** Geonwook Kim[1], Hyunho Seok[2], Sihoon Son[3], Hyunbin Choi[4], Jinhyoung Lee[1], Dongho Lee[1], Seowoo Son[3], and Taesung Kim[1,3,4] [1]School of Mechanical Engineering, Sungkyunkwan University, [2]Research Laboratory of Electronics, MIT, [3]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University, [4]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
TD3-K-6 15:30-15:45	**Vertical Ferroelectric Tunnel Junctions with Composition-Tuned Oxide Semiconductors for Enhanced TER and Self-Rectifying Behavior** Yeonwoo Choi[1], Kyungsoo Park[2], Jin Yeong Lee[1], Taesuk Kim[2], Sang Myun Lim[1], Jihoon Choi[1], Hyeoncheol Jeong[1], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University

2026년 1월 29일(목), 14:00-15:45
Room E(5층, 에메랄드)

P. Device for Energy (Solar Cell, Power Device, Battery, etc.) 분과

O51_[TE3-P] Electrochemical Energy Device

좌장: 주종훈 교수(GIST), 김선동 박사(한국에너지기술연구원)

초청발표 **TE3-P-1** 14:00-14:30	**Solid Oxide Electrolysis Cells for Clean Hydrogen Production** Sun-Dong Kim[1,2] [1]High Temperature Electrolysis Laboratory, Korea Institute of Energy Research, [2]National Hydrogen Hub Laboratory for SOEC
TE3-P-2 14:30-14:45	**Dual Synergistic Effects of SOCs ALD CeO_2 Infiltration PrOx@LSCF Oxygen Electrode for Enhanced Catalyst Activity and Stability** Woojin Park, Hyongjune Kim, and Jihwan An Department of Mechanical Engineering, POSTECH
TE3-P-3 14:45-15:00	**Composition-Controlled Cathode Protective Layer via Powder-Atomic Layer Deposition for All-Solid-State Batteries** Kyu Moon Kwon[1], Dae Ho Kim[1], Ha Yeon Kwon[1], Joungwon Park[2], Kyoung Hwan Kim[2], Hwi-Yeol Park[2], Hyo Rang Kang[1,3], and Tae Joo Park[1,4] [1]Department of Materials Science & Chemical Engineering, Hanyang University, [2]Battery Material TU, Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd., [3]NanoCamp Inc., [4]ALPES Co., Ltd.
TE3-P-4 15:00-15:15	**Atomic Scale Tracking of Li Ion Migration in Epitaxial T-Nb_2O_5 Using In situ STEM** Sol-I Sung[1], Yaolong Xing[1,2], Jinho Byun[1], Hyun Han[3,4], and Sang Ho Oh[1] [1]Department of Energy Engineering, KENTECH, [2]Max Planck Institute for Sustainable Materials, [3]Department of Materials Science and Engineering, POSTECH, [4]Max Planck Institute of Microstructure Physics
TE3-P-5 15:15-15:30	**Thin Film Ion-selective Hydrogel Separator for Sodium Resource Utilization and Adaptive Energy Storage** Hyunlee Kim[1], Hyewon Song[2], Do Hyeon Jung[2], Chuong Van Ho[2], Hui Hun Cho[2], Jun Hyuk Heo[2], and Jung Heon Lee[1,2] [1]Department of MetaBioHealth, Sungkyunkwan University, [2]School of Advanced Materials Science and Engineering, Sungkyunkwan University
TE3-P-6 15:30-15:45	**Enhancing Interfacial Stability of Li Metal Anodes via In-situ H_2 Plasma Surface Treatment and a Low-Temperature Lithicone Passivation Layer** Ha Yeon Kwon[1], Kyu Moon Kwon[1], Min Jung Choi[1], Syed Jazib Abbas Zaidi[1], Seung Jeong Oh[2], Hyo Rang Kang[1,3], and Tae Joo Park[1] [1]Department of Materials Science & Chemical Engineering, Hanyang University, [2]R&D Division, Hyundai Motors Co., Ltd., [3]NanoCamp Inc.

2026년 1월 29일(목), 14:00-15:45
Room F(5층, 사파이어)

C. Material Growth & Characterization 분과

O52_[TF3-C] 2D vdW Semiconductors and Heterostructures

좌장: 이정우 교수(홍익대학교), 백승협 책임박사(KIST)

TF3-C-1 14:00-14:15	**Geometrically Induced Boundary Layer Propel Wafer-Scale Monolayer Tungsten Disulfide Synthesis** Dongho Lee[1], Seowoo Son[2], Hyunho Seok[3], Hyunbin Choi[4], Geon Wook Kim[1], and Taesung Kim[1,2,4] [1]School of Mechanical Engineering, Sungkyunkwan University, [2]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University, [3]Research Laboratory of Electronics, MIT, [4]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
TF3-C-2 14:15-14:30	**Hidden Ferroelectricity Unlocked in Centrosymmetric WS_2 Bilayers** Seowoo Son[1], Dongho Lee[2], Hyunho Seok[3], Jinhyoung Lee[2], Gunhyeong Kim[4], Sihoon Son[1], Hyunbin Choi[4], Geonwook Kim[2], and Taesung Kim[1,2,4] [1]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University, [2]School of Mechanical Engineering, Sungkyunkwan University, [3]Research Laboratory of Electronics, MIT, [4]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
초청발표 **TF3-C-3** 14:30-15:00	**Phase-Tunable Growth of van der Waals Semiconductors: 2D $MoTe_2$ and InSe Systems for Logic and Reconfigurable Nanoelectronics** Seunguk Song[1,2] [1]Department of Energy Science, Sungkyunkwan University, [2]Center for 2D Quantum Heterostructures, IBS, Sungkyunkwan University
초청발표 **TF3-C-4** 15:00-15:30	**Epitaxially Assembled van der Waals Heterostructures for In-sensor Computing** 서준기 KAIST
TF3-C-5 15:30-15:45	**Atomic-Level Conformal-Growth-Enabled Monolithic Integration of Vertical Monolayer MoS_2 Field-Effect Transistor** Seonguk Yang[1], Huimin Lee[2], Hanbin Cho[1], Ki Han Kim[3], Saeyoung Oh[2], Hoyeon Cho[4], Kyungmin Ko[4], Namwook Hur[4], Hu Young Jeong[2], Byung Chul Jang[3], and Joonki Suh[1] [1]Department of Chemical and Biomolecular Engineering, KAIST, [2]Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [3]School of Electronic and Electrical Engineering, Kyungpook National University, [4]Department of Materials Science and Engineering, UNIST

2026년 1월 29일(목), 14:00-15:45
Room G(5층, 루비 II)

N. VLSI CAD 분과

O53_[TG3-N] Advanced CAD for VLSI

좌장: 현대준 교수(세종대학교), 박희천 교수(UNIST)

초청발표 **TG3-N-1** 14:00-14:30	**Design Methodologies for Memory: Design Implementation Perspective** 안세용 삼성전자 메모리사업부
TG3-N-2 14:30-14:45	**Logic Partitioning Methodology for Utilizing Active Backside Layers** Minhong Kim, Ikkyum Kim, and Heechun Park Department of Electrical Engineering, UNIST
TG3-N-3 14:45-15:00	**Dataflow-aware Placement Optimization for Digital Compute-in-Memory (DCIM) Using H-Tree-Like Adder Tree Organization** Mingyeom Kim[1], Gangmin Jeon[2], and Heechun Park[2] [1]Kookmin University, [2]UNIST
TG3-N-4 15:00-15:15	**PPA-Driven Multi-Bit Flip-Flop Clustering based on Minimum-Cost Maximum-Flow Algorithm** Jiyun Ham, Sojung Park, and Heechun Park UNIST
TG3-N-5 15:15-15:30	**Monte Carlo Tree Search with LLM for Design Space Optimization** Jongho Yoon, Jeonghyun Choi, and Seokhyeong Kang Department of Electrical Engineering, POSTECH
TG3-N-6 15:30-15:45	**ILP-Based Pad Assignment for Signal and Power Integrity** Hyuk Ko and Daijoon Hyun Department of Semiconductor Systems Engineering, Sejong University

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Room H(6층, 스페이드)

G. Device & Process Modeling, Simulation and Reliability 분과

O54_[TH3-G] Device & Process Modeling, Simulation and Reliability V

좌장: 이영훈 교수(인천대학교), 백록현 교수(POSTECH)

TH3-G-1 14:00-14:15	**Quantum Transport Simulation for a-IGZO Channel Devices Considering Structural Disorder Effect** Jooseok Kim[1], Ilhan Yu[1], Gyeongwon Roh[1], Yeongjun Lim[1], Seonghyun Kim[2], Hyejung Choi[2], Soogil Kim[2], and Mincheol Shin[1] [1]School of Electrical Engineering, KAIST, [2]Component Research, R&D Division, SK hynix Inc.
TH3-G-2 14:15-14:30	**Numerically Stable Compact Model of a Bistable Resistor (Biristor) for Circuit and Array-Level Applications** Hanbin Lee[1], Ji Won Park[1], Seonghyeon Jeong[1], Jeong Yeon Im[1], So-Jeong Park[1], Youngmin Kim[1], Yoon Jung Lee[1], Dae Hwan Kim[1], Jihoon Han[2], Seheon Oh[2], Youngchul Kim[2], and Sung-Jin Choi[1] [1]School of Electronics and Electrical Engineering, Kookmin University, [2]ESD/TCAD Team, Technology Enabling Center, DB HiTek
TH3-G-3 14:30-14:45	**Exploring Layer Number-Dependent Hole Transport in W- and Mo-Based Two-Dimensional Materials via Full-Band Semi-Classical Monte Carlo Simulation** Donghyeok Lee[1], Sukhyeong Youn[1], and Jiwon Chang[1,2] [1]Department of Materials Science and Engineering, Yonsei University, [2]Department of System Semiconductor Engineering, Yonsei University
TH3-G-4 14:45-15:00	**TCAD Fast 3D Calibration Method to Analysis Edge Terminal in LDMOS** Jihye Park, Jieen Lee, Jong Min Kim, Young Chul Kim, and Hyunchul Nah ESD/TCAD Team, Technology Enabling Center, DB HiTek
TH3-G-5 15:00-15:15	**Impact of Post-Channel-Release SiGe Residue in Forksheet FETs** Sunmin Yeou, Sanguk Lee, Jongseo Park, Yonghwan Ahn, Minchan Kim, Gunryeol Cho, and Rock-Hyun Baek Department of Electrical Engineering, POSTECH
TH3-G-6 15:15-15:30	**TCAD-Guided Calibration of Compact Models for IGZO TFTs in 6T1C Synaptic Memory Applications** Ye-Han Kwon, Seung-Woo Jung, and Sung-Min Hong Department of Electrical Engineering and Computer Science, GIST
TH3-G-7 15:30-15:45	**Degradation Behavior of NPN BJTs under On/Off Collector Stress Conditions** Ju-Yong Shin, Yu-Bin Kim, Ju-Han Lee, and Hi-Deok Lee Department of Electronics Engineering, Chungnam National University

2026년 1월 29일(목), 14:00-15:45
Room I(6층, 하트)

F. Silicon and Group-IV Devices and Integration Technology 분과

O55_[TI3-F] GAA/CFET Device Technology and Design

좌장: 김명수 교수(UNIST), 황현준 교수(목포대학교)

TI3-F-1 14:00-14:15	**Design Technology Co-Optimization (DTCO): Performance Analysis of Gate Extension Scaling on Nanosheet FET Considering Gate Metal Work-Function Non-Uniformity** Jung Su Kim and Changhwan Shin School of Electrical Engineering, Korea University
TI3-F-2 14:15-14:30	**Uniaxially Compressively Strained Ge (100)-OI p-MOSFET for High-Performance 3D Stacked FET (3DSFET) Applications** Hyeongrak Lim[1], Seong Kwang Kim[1], Hojin Jeong[1], Jinha Lim[1], Songhyeon Kuk[1], Dae-Myeong Geum[2], Jinho Bae[3], Jaehyun Park[3], Daewon Ha[3], Jaehoon Han[4], Younghyun Kim[5], Jaeyong Jeong[1], and Sanghyeon Kim[1] [1]KAIST, [2]Inha University, [3]Semiconductor R&D Center, Samsung Electronics Co., Ltd., [4]KIST, [5]Hanyang University
TI3-F-3 14:30-14:45	**그린 레이저 열처리 공정 도입을 통한 상부 Ge PMOS 기반 이종 3차원 순차적 CFET 성능 개선** 박영근, 임형락, 정재중, 김준표, 김성광, 김상현, 조병진 한국과학기술원 전기 및 전자공학부
TI3-F-4 14:45-15:00	**Comparative Analysis of Rare-Earth Elements (La, Y, Gd) Oxides Based Dipole-First Gate Stack for Multi-Vt Design Integration Targeting Low Thermal Budget CFET Device** Sangkuk Han[1], Wonjae Choi[2], Jaewon Chung[2], Haesoo Jang[2], Kyungwook Park[1], Sangmyun Lim[2], Soyoung Park[2], Sangwoo Jeong[1], Hanbyul Kim[3], Yong Joo Park[3], and Changhwan Choi[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University, [3]SK Trichem Co., Ltd.
TI3-F-5 15:00-15:15	**Process Emulation and Device Simulation of Three-Dimensional Complementary Transistor Architecture, Flip FET** Min-Seo Jang and Sung-Min Hong Department of Electrical Engineering and Computer Science, GIST
TI3-F-6 15:15-15:30	**고품질 헤테로 에피 기반으로 구현된 GAA-FET 소자 특성** 이성현, 김진하, 김상훈, 박민아, 정순규, 손민균, 김지은, 허수빈, 박재성, 최석원, 송한찬, 이왕주, 구스타보 파나마, 임종필, 박소영, 박정우, 서동우 한국전자통신연구원 인공지능창의연구소 소재부품연구본부
TI3-F-7 15:30-15:45	**Lattice Kinetic Monte Carlo (LKMC) Simulation to Investigate the Impact of Growth Size of Epitaxial-Source/Drain on the Drive Current of NSFET** Hyunwoo Lee and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University

2026년 1월 29일(목), 14:00-15:45
Room J(6층, 다이아몬드)

H. Display and Imaging Technologies 분과

O56_[TJ3-H] Emerging Displays and Image Sensors

좌장: 정예환 교수(한양대학교), 백근우 교수(한밭대학교)

초청발표 **TJ3-H-1** 14:00-14:30	**Strategy for Simultaneous Strain-Engineering and Chip Bonding for Stretchable Display and Electronics Applications** Yongtaek Hong[1,2] [1]Department of Electrical and Computer Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University
초청발표 **TJ3-H-2** 14:30-15:00	**Natural Strategies for Vision: Inspiring Advanced Robotic Imaging Systems** Young Min Song School of Electrical Engineering, KAIST
TJ3-H-3 15:00-15:15	**Stretchable Display with Cellulose Nanocrystal-Based Optical Diffuser for Strain-Invariant Image Quality** Kyung Jun Lee[1], Hyeon Ho Shin[2], and Yei Hwan Jung[1,2] [1]Department of Artificial Intelligence Semiconductor Engineering, Hanyang University, [2]Department of Electronic Engineering, Hanyang University
TJ3-H-4 15:15-15:30	**Enhanced Thermal and Optical Performance in Vertically Stacked μLEDs via Oxide-Based Wafer Bonding** Hyun Soo Kim, Juhyuk Park, Woo Jin Baek, and SangHyeon Kim School of Electrical Engineering, KAIST
TJ3-H-5 15:30-15:45	**Low-Voltage Resonant Reflective Display via MOSFET-Assisted Selective Pixel Deposition** Jun Seo Lee[1], Jae Min Jeon[1], Hyo Eun Jeong[2], and Young Min Song[2] [1]School of Electrical Engineering and Computer Science, GIST, [2]School of Electrical Engineering, KAIST

2026년 1월 29일(목), 15:55-17:40
Room A(4층, 그랜드볼룸 I+II)

D. Thin Film Process Technology 분과

O57_[TA4-D] Emerging Devices III

좌장: 손준우 교수(서울대학교), 백인환 교수(인하대학교)

TA4-D-1 15:55-16:10	**Reversible Gap State Saturation of MoS_2-Semimetal Interface for Uninterrupted Synaptic Weight** 손시훈[1,2], 최현빈[3], 김건욱[4], 김태성[1,2,3,4] [1]성균관대학교 나노과학기술학과, [2]성균관대학교 SKKU Advanced Institute of Nano Technology, [3]성균관대학교 반도체융합공학과, [4]성균관대학교 기계공학과
TA4-D-2 16:10-16:25	**One-Shot Remote Integration of Polymer Synaptic Arrays for Flexible Neural Network System** Jaehoon Lee[1], Jihun Noh[2], Sungmo Kang[1], and Bosoek Kang[1,2] [1]Department of Nanoscience and Technology, Sungkyunkwan University, [2]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
TA4-D-3 16:25-16:40	**Ferroelectric Synaptic Transistors with Tunable Plasticity via Coupled Gate-Insulator and Active-Layer Engineering** Ji-Won Jang, Hyun-Sik Kim, Hong-Sub Lee, and Sung-Min Yoon Kyung Hee University
TA4-D-4 16:40-16:55	**Reconfigurable Floating-Gate Memory based on van der Waals Heterostructures** Seongwook Yoon[1] and Woo Jong Yu[2] [1]Department of Semiconductor Convergence Engineering, Sunkyunkwan University, [2]Department of Electrical and Computer Engineering, Sungkyunkwan University
TA4-D-5 16:55-17:10	**Gate Insulator Stack Engineering for Simultaneous Enhancement of On-Current and Reliability in a-IGZO TFT-Based Synaptic Circuits** Youngchae Roh[1,2,3], Narae Han[1,4], Ha-jun Sung[4], Sangbum Kim[1,2,3], Sangwook Kim[4], Minseung Kang[1,2,3], Jongun Won[1,2,3], Joo-Hun Han[4], Younjin Jang[4], and Jee-Eun Yang[4] [1]Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University, [3]Research Institute of Advanced Materials, Seoul National University, [4]Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd.
TA4-D-6 17:10-17:25	**Impact of Neutron Irradiation on α-In_2Se_3 Ferroelectric Memory under Harsh Environments** Sieun Lee[1], Jaewook Yoo[2], Hongseung Lee[2], Seongbin Lim[2], Minah Park[2], Seohyeon Park[2], Sojin Jung[2], Donghyeon Lee[2], Soohyun Lim[2], Dongsun Shin[2], Junhui Park[2], Bong-ki Jung[3], Taewan Kim[4], and Hagyoul Bae[2] [1]Department of Electrical Engineering, Jeonbuk National University, [2]Department of Electronic Engineering, Jeonbuk National University, [3]Q-beam solution Inc., [4]Department of Intelligent Semiconductor Engineering, University of Seoul
TA4-D-7 17:25-17:40	**Bi-Heterojunction Noise-Enhanced Transistors for Multi-Bit Stochasticity and Secure Image Generation** Youngmin Han[1], Jaechan Song[2], and Hocheon Yoo[1] [1]Department of Electronic Engineering, Hanyang University, [2]Department of Artificial Intelligence Semiconductor Engineering, Hanyang University

2026년 1월 29일(목), 15:55-17:40
Room B(4층, 그랜드볼룸 III)

B. Patterning (Lithography & Etch Technology) 분과

O58_[TB4-B] Advanced Etch

좌장: 김규현 전문교수(SK hynix), 김재호 교수(성균관대학교)

초청발표 **TB4-B-1** 15:55-16:25	**Dry Etching 장비의 발전 맥락과 차세대 Etching 기술 개발** Jong Chul Park Semiconductor R&D Center, Samsung Electronics Co., Ltd.
TB4-B-2 16:25-16:40	**Low Temperature Etch of Silicon Oxide Using Ar/CF_4/H_2O Plasma** Hakseung Lee[1,2], Haegeon Jung[1,2], Kangwoo Lee[3], Daeun Hong[3], Minsung Jeon[4], and Heeyeop Chae[3,4] [1]Department of Semiconductor Display Engineering, Sungkyunkwan University, [2]Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd., [3]School of Chemical Engineering, Sungkyunkwan University, [4]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
TB4-B-3 16:40-16:55	**Optimized hBN Spacer Thickness in Plasmonic WSe_2/AuNPs Photodetectors: An Experimental and Computational Study** 이수빈, 김지현 서울대학교 화학생물공학부
TB4-B-4 16:55-17:10	**Investigation of Area-Selective Ru Deposition via Substrate-dependent ALD-Etch Supercycles** Youngseo Na[1], Hyunjin Lim[2], Seungchae Lee[2], Yehbeen Im[2], Donguk Kim[1], Kangbaek Seo[1], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University
TB4-B-5 17:10-17:25	**C=C 결합이 포함된 C_3HF_5와 C_3F_6 플라즈마의 SiO_2 식각** 조인경[1,2], 김창구[1,2] [1]Department of Chemical Engineering, Ajou University, [2]Department of Energy Systems Research, Ajou University
TB4-B-6 17:25-17:40	**Influence of Oxygen and HBr on the Etching Characteristics of Molybdenum Thin Films in Cl_2/O_2/HBr/Ar Gas Mixture** Hong Ju Yang[1,2], Jae Min Jung[1,2], Ho Jin Jung[1,2], In-Hwan Baek[1,2], and Chee Won Chung[1,2] [1]Department of Chemical Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University

2026년 1월 29일(목), 15:55-17:40
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O59_[TC4-D] Thin Film Transistors II

좌장: 최창환 교수(한양대학교), 오일권 교수(아주대학교)

TC4-D-1 15:55-16:10	**Vertically Integrated Stacking InGaZnO Vertical Thin-Film Transistors with Shared Channel for Scalable Monolithic 3D Integration** Young-Jae Kim[1], Ji-Won Kang[1], Chi-Sun Hwang[2], and Sung-Min Yoon[1] [1]Kyung Hee University, [2]ETRI
TC4-D-2 16:10-16:25	**Gate-Stack Engineering of Vertical-Channel Charge-Trap Memory Transistors with ALD-IGZO Channel for High-Density Nonvolatile Storage** Yu-jin Jung[1], Kyung-Min Kim[1], Chi-Sun Hwang[2], and Sung-Min Yoon[1] [1]Kyung Hee University, [2]ETRI
TC4-D-3 16:25-16:40	**Material-Driven Formation of Two-Dimensional Electron Gas at In_2O_3/Al_2O_3 Interfaces with Atomic Layer Deposition** Kyunghun Lyu, Jiyoung Park, Jiwon Ahn, and Woongkyu Lee Department of Materials Science and Engineering, Soongsil University
TC4-D-4 16:40-16:55	**Analysis of Hysteresis in MoS_2 Field Effect Transistor via Surface Engineering Using Low-Frequency O_2 Plasma Treatment** Seung Ri Jeong, Ha Yeon Choi, Joon Soo Byeon, Ju Yong Shin, Jong Mun Park, Shivam Kumar Gautam, and Hi Deok Lee Department of Electronics Engineering, Chungnam National University
TC4-D-5 16:55-17:10	**Low-Temperature Process Strategies for High-Performance BEOL-Compatible p-Type SnO Thin-Film Transistors** Jaemin Jeong[1,2], Jaeyoon Shim[1,2], Dahui Jeon[1,2], Sung Kwang Lee[3], Taek-mo Chung[3], and In-Hwan Baek[1,2] [1]Department of Chemical Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University, [3]Division of Advanced Materials, KRICT
TC4-D-6 17:10-17:25	**Scavenging-Driven Interface Engineering for High-Performance Te-Based p-Type TFTs via ALD Al_2O_3 Passivation** Jaeyoon Shim[1,2], Jaemin Jung[1,2], Dahui Jeon[1,2], and In-Hwan Baek[1,2] [1]Department of Chemical Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University
TC4-D-7 17:25-17:40	**P-Type Tellurium Thin Film Transistor with Sacrificial Atomic Layer Deposition** Wonho Choi[1,2], Byongwoo Park[1,2], Seungjae Yoon[1,2], Gwangsik Jeon[1,2], Sangmin Jeon[1,2], Sungjin Kim[1,2], Junwoo Park[1,2], and Cheol Seong Hwang[1,2] [1]Department of Materials Science and Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University

2026년 1월 29일(목), 15:55-17:40
Room D(5층, 컨벤션홀 L)

K. Memory (Design & Process Technology) 분과

O60_[TD4-K] Advanced Memory

좌장: 김태현 교수(서울과학기술대학교), 정연주 책임(KIST)

초청발표 **TD4-K-1** 15:55-16:25	**RRAM and Flash AND Array Platform for Energy-Efficient Spiking Neural Network Computation** Sungjun Kim Division of Electronics and Electrical Engineering, Dongguk University
TD4-K-2 16:25-16:40	**Experimental Demonstration of Configurable Kernel Mapping in Memristor Crossbar for Convolutional Neural Networks** Sangwook Youn[1,2], Jinwoo Park[1,2], and Hyungjin Kim[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University
TD4-K-3 16:40-16:55	**Advances and Perspectives of Selector-Only Memory (SOM) for Future Memory Applications** 연정호, 반상현, 최혜정, 김명섭, 김수길, 이재연, 차선용 SK hynix Inc.
TD4-K-4 16:55-17:10	**Bi-Based Selector Only Memory for High-Density 3D Stacked Memory** Chang Deok Han, Su Yong Chae, and Seung Hwan Lee Department of Semiconductor Engineering, Kyung Hee University
TD4-K-5 17:10-17:25	**Identical Pulse Based Compensation Resistors for Linear Potentiation and Depression of Synaptic Device** Minsu Kang[1], Sion Kim[1], Yuna Kim[1], Eungcheol Kim[2], Sarah Yoon[2], Songye Lim[2], and Daeseok Lee[1] [1]School of Semiconductor System Engineering, Kwangwoon University, [2]Department of Electronic Materials Engineering, Kwangwoon University
TD4-K-6 17:25-17:40	**Electrical Properties Between Chalcogenide Ovonic Threshold Switch and Metal Electrodes** MiRiNae Lee[1,2], Junghoon Han[1,3], ChaHwan Yang[1,2], Kyunghee Choi[1], and Sooji Nam,[1,2] [1]Department of Electric Engineering, ETRI, [2]Semiconductor and Advanced Device Engineering, University of Science and Technology, [3]Department of Micro/Nano Systems, Korea University

2026년 1월 29일(목), 15:55-17:10
Room E(5층, 에메랄드)

P. Device for Energy (Solar Cell, Power Device, Battery, etc.) 분과

O61_[TE4-P] 전력반도체 소자

좌장: 홍영준 교수(성균관대학교), 김형탁 교수(홍익대학교)

초청발표 **TE4-P-1** 15:55-16:25	**질화갈륨 전력반도체소자의 다양한 열화현상과 메커니즘** 김형탁 홍익대학교 전자전기공학부
TE4-P-2 16:25-16:40	**Monolithic Growth of AlGaAs/Si Tandem Solar Cells with a High Bandgap 1.7 eV n-AlGaAs Buffer on GaP/Si** Yeonhwa Kim[1,2], Tsimafei Laryn[1,3], In-Hwan Lee[2], Won Jun Choi[1], and Daehwan Jung[1,3] [1]Center for Quantum Technology, KIST, [2]Department of Materials Science and Engineering, Korea University, [3]Division of Nanoscience and Technology, KIST School at University of Science and Technology
TE4-P-3 16:40-16:55	**반도체 패키지 방열 품질 관리를 위한 확률론적 열 구조 함수** 송원빈[1], 이규석[2], 윤병동[1,3] [1]서울대학교 기계공학과, [2]한국전자기술연구원 신뢰성연구센터, [3]원프레딕트
TE4-P-4 16:55-17:10	**Flexible InGaP/GaAs/InGaAs 3J Solar Cell for Unassisted Photocatalysis and Space Applications** Sukkyu Hong[1,2], Seungwan Woo[1], Hyun-Beom Shin[3], Ho Kwan Kang[3], Jeongeun Mo[1], Sung-Min Lee[2], and Won Jun Choi[1] [1]Center for Quantum Technology, KIST, [2]Department of Electrical Engineering, Hanyang University, [3]KANC

2026년 1월 29일(목), 15:55-17:40
Room F(5층, 사파이어)

A. Interconnect & Package 분과

O62_[TF4-A] Advanced Package III

좌장: 박아영 교수(서울시립대학교), 김명준 교수(성균관대학교)

초청발표 **TF4-A-1** 15:55-16:25	**Packaging-Driven Reliability Divergence in Power MOSFETs: Insights from Single-Die and Cascode Stack-Die Devices** You-Cheol Jang Global R&D Center, HL Mando
TF4-A-2 16:25-16:40	**Study of Substrate-Dependent Signal Integrity in Chiplet Systems** Yurim Choi[1], Yongwoo Lee[1], Haksoon Jung[2], and Jimin Kwon[1,2] [1]Department of Electrical Engineering, UNIST, [2]Graduate School of Semiconductor Materials and Devices Engineering, UNIST
TF4-A-3 16:40-16:55	**3D-Printed 28-GHz Antenna-in-Package Lid Substrate Featuring 50-Ohm Quasi-Coaxial Through-Vias** Nahyeon Kim[1], Kyungsun Kim[1], Haksoon Jung[2], and Jimin Kwon[1,2] [1]Graduate school of Semiconductor Materials and Devices Engineering, UNIST, [2]Department of Electrical Engineering, UNIST
TF4-A-4 16:55-17:10	**Heat Transfer Modeling for High-Performance Semiconductor Package Using Finite Element Analysis: Experimental Validation and Deep Learning-Based Approach for Acceleration** Min-Jun Cheon[1], Seongjin Kim[2], Jung-Won Lee[3], Lewis Kang[3], Sungmo Kang[4], Inhak Han[5], Jae Yong Song[2], and Hoon-Hwe Cho[1] [1]Hanbat National University, [2]POSTECH, [3]Nepes, [4]Asicland Co., Ltd., [5]Baum
TF4-A-5 17:10-17:25	**A Validated Multi-Scale Framework for Predicting the Effective Thermal Conductivity of Cu-BAs Composites for Advanced Packaging Applications** Hyunwoo Jung[1], Ki-Han Lee[1], Sung-Jun Kang[1], Seolim Yoon[1], Jongchan Park[1], Jaehoon Kim[2], Minjeong Sohn[3], Tae-Ik Lee[3], Joon Sang Kang[2], Myung Jun Kim[1], and Eun-Ho Lee[1] [1]Sungkyunkwan University, [2]KAIST, [3]KITECH
TF4-A-6 17:25-17:40	**Characterization of AlN Powder Thermal Conductivity for Thermal Interface Material** Jinwook Lee[1,2], Jaewoo Lee[1,2], Taeheun Lim[1,2], Jungyoon Hur[1,2], Heesoo Lee[1,2], and Woo Jin Kim[1,2] [1]Department of Materials Science and Engineering, Pusan National University, [2]Institute of Materials Technology, Pusan National University

2026년 1월 29일(목), 15:55-17:40
Room G(5층, 루비 II)

N. VLSI CAD 분과

O63_[TG4-N] Machine Learning for Electronic Design Automation

좌장: 현대준 교수(세종대학교), 박희천 교수(UNIST)

TG4-N-1 15:55-16:10	**Multi-Objective Logic Optimization with Diffusion Model** Jiwon Kang[1], Dhoui Lim[2], and Heechun Park[2] [1]School of Electronics and Electrical Engineering, Hongik University, [2]Department of Electrical Engineering, UNIST
TG4-N-2 16:10-16:25	**Enhancing Timing Closure via Spatially Embedded Graph Transformer with Low Power/Area Overhead** Hyunjung Cho, Joonyoung Seo, and Seokhyeong Kang Department of Electrical Engineering, POSTECH
TG4-N-3 16:25-16:40	**Timing-Driven Hierarchical Gate Sizing with Reinforcement Learning** Kijung Kong, Geonhyeong Park, and Heechun Park Department of Electrical Engineering, UNIST
TG4-N-4 16:40-16:55	**Physical-Aware Diffusion Model for Macro Placement** Jongho Yoon, Yunjun Nam, and Seokhyeong Kang Department of Electrical Engineering, POSTECH
TG4-N-5 16:55-17:10	**A Heterogeneous Graph and Transformer-Based Approach to Gate Sizing for PPA Improvement** Mungyu Choi, Jinmo Ahn, and Seokhyeong Kang Department of Electrical Engr., POSTECH
TG4-N-6 17:10-17:25	**LLM-Based RTL Generation and PPA Improvement Using Evolutionary Computation** Hayoung Shin, Kyungjun Min, Kyumin Cho, and Seokhyeong Kang Graduate School of Semiconductor Technology, POSTECH
TG4-N-7 17:25-17:40	**Post-Route Timing Prediction from Synthesis-Level Netlists Using a Graph Neural Network** Hyeon Jeong Lee and Suwan Kim Department of Electronic Engineering, Kyung Hee University

2026년 1월 29일(목), 15:55-17:40
Room H(6층, 스페이드)

E. Compound Semiconductors 분과

O64_[TH4-E] Reliability and Radiation Hardness

좌장: 차호영 교수(홍익대학교), 석오균 교수(부산대학교)

초청발표 **TH4-E-1** 15:55-16:25	**Charge Trapping as a Design Opportunity and a Reliability Challenge in GaN HEMTs** Junseok Heo[1,2] [1]Department of Intelligence Semiconductor Engineering, Ajou University, [2]Department of Electrical and Computer Engineering, Ajou University
TH4-E-2 16:25-16:40	**E-mode GaN 트랜지스터에서 게이트 전압에 의한 문턱전압 양의 변화의 게이트 누설 전류 영향 분석** 채명수, 김형탁 홍익대학교 전자전기공학부
TH4-E-3 16:40-16:55	**Radiation Tolerance Improvement in GaN-Based HEMTs Using Extremely Thin h-BN Passivation Layer and Air Spacer** Sung-Jae Chang[1], Seokho Moon[2], Junhyung Jeong[1], Hyun-Wook Jung[1], Ho-Kyun Ahn[1], Dong-Min Kang[1], Jong Kyu Kim[2], Jong-Won Lim[1], and Dong-Seok Kim[3] [1]Photonic/Wireless Convergence Research Department, ETRI, [2]Department of Materials Science and Engineering, POSTECH, [3]Korea Multi-purpose Accelerator Complex, KAERI
TH4-E-4 16:55-17:10	**High-Temperature and Radiation Effects on Al-Rich AlGaN Channel HEMTs with Various Gate Metals** Mingoo Jo[1,2], Joocheol Jeong[1,2], Shyam Mohan[1,2], Jaejin Heo[1,2], Hyogeun Cho[1,2], Minyeong Kim[1,2], Dongseok Kim[3], and Okhyun Nam[1,2] [1]Convergence Center for Advanced Nano Semiconductor, Tech University of Korea, [2]Department of Semiconductor Engineering, Tech University of Korea, [3]Korea Multi-purpose Accelerator Complex, KAERI
TH4-E-5 17:10-17:25	**Electrical Characteristics of H-Diamond FETs with Al/Al_2O_3/Al Gate under Proton Irradiation** Hyunsu Ma[1], Taemyung Kyak[1], Yoonseok Nam[1], Geunho Yoo[1], Dongseok Kim[2], Seong-woo Kim[3], and Okhyun Nam[1] [1]Convergence Center for Advanced Nano Semiconductor, Department of Nano-Semiconductor Engineering, Tech University of Korea, [2]KAERI, [3]Obray Co., Ltd.
TH4-E-6 17:25-17:40	**Effect of Gamma(γ)-Ray Radiation on Tin Oxide Field-Effect Transistors** Seonchang Kim[1], Huiseung Kim[2], Jeongtae Kim[1], Roy Byung Kyu Chung[2], and Dong-Seok Kim[1] [1]Korea Multi-purpose Accelerator Complex, KAERI, [2]Department of Electronic Science and Engineering, Kyungpook National University

2026년 1월 29일(목), 15:55-17:40
Room I(6층, 하트)

Q. Metrology, Inspection, Analysis, and Yield Enhancement 분과

O65_[TI4-Q] Metrology, Inspection, Analysis, and Yield Enhancement II

좌장: 김경태 책임연구원(나노종합기술원), 박인용 박사(한국표준과학연구원)

초청발표 **TI4-Q-1** 15:55-16:25	**Next-Generation Digital 3D X-ray CT Metrology for Advanced Semiconductor Structures** Jehwang Ryu CAT Beam Tech Co., Ltd.
초청발표 **TI4-Q-2** 16:25-16:55	**HBM Stacking Process 발전과 Stacking Misalignment Metrology** Hyunjin Chang AUROS Technology Inc.
TI4-Q-3 16:55-17:10	**OCD Spectrum-Based Anomaly Index for Process Evaluation of High-Aspect-Ratio Structures in V-NAND Devices** Hoyeon Kim[1], Sohee Han[1], Seong Yun[1], Eonho Park[1], JunWoong Hur[1], Eunseo Choi[2], Heejin Ahn[2], Jaewon Lee[1], Taeyong Jo[1], and Myungjun Lee[1] [1]Advanced Process Development Team, Samsung Electronics Co., Ltd., [2]School of Electrical Engineering, KAIST
TI4-Q-4 17:10-17:25	**A Compact Actinic EUV Exposure Platform for Quantitative Photoresist Evaluation Using Femtosecond HHG EUV Source** Hyuk Jin Kim[1], Geonhwa Kim[1], Namhyeon Kim[1], Boknam Chae[1], Yejin Ku[3], Gayoung Kim[3], JinKyun Lee[3], Jiho Kim[1], and Sangsul Lee[1,2] [1]Pohang Accelerator Laboratory, POSTECH, [2]Department of Semiconductor Engineering, POSTECH, [3]Department of Polymer Science and Engineering, Inha University
TI4-Q-5 17:25-17:40	**Flare-Integrated Evaluation Methodology for High-NA EUV Pellicle with Precise Transmission-Reflection Measurements** Geonhwa Kim[1], Jiho Kim[1], Namhyeon Kim[1], Hyuk Jin Kim[1], Byeong-Gyu Park[1], Jeong Kyu Kim[1], and Sangsul Lee[1,2] [1]Pohang Accelerator Laboratory, POSTECH, [2] Department of Semiconductor Engineering, POSTECH

2026년 1월 29일(목), 15:55-17:25
Room J(6층, 다이아몬드)

H. Display and Imaging Technologies 분과

O66_[TJ4-H] Thin Film Transistors for Displays II

좌장: 정예환 교수(한양대학교), 노정균 교수(부산대학교)

초청발표 **TJ4-H-1** 15:55-16:25	**Submicron Channel Length Oxide Semiconductor Thin-Film Transistors with Top-Gate and Self-Aligned Process Architecture and Their Monolithic Integration on Si CMOS Wafer** Sung Haeng Cho, Chihun Sung, and Jeho Na Flexible Electronics Research Section, ETRI
TJ4-H-2 16:25-16:40	**Extremely Flexible MOSFETs with Micrometer-Scale Radius of Curvature in Flexible Display Backplanes** Chang Hyeon Park and Yei Hwan Jung Department of Artificial Intelligence Semiconductor Engineering, Hanyang University
TJ4-H-3 16:40-16:55	**Swing-Tunable Thin-Film Transistors for Improved Low-Gray-Scale OLED Operation** Jae Won Na ETRI
TJ4-H-4 16:55-17:10	**Engineering SiNx Gate Insulators via Precursor Ligand Chemistry for High-Performance IGZO TFTs** YuJin Yang[1], Sang-Hyun Kim[2], and Jin-Seong Park[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Department of Display Science and Engineering, Hanyang University
TJ4-H-5 17:10-17:25	**A Novel AMOLED Display Pixel Circuit for Reducing Leakage Current Induced by Kickback Voltage** Dae Cheol Ha[1], Kook Chul Moon[2], and Yong-Sang Kim[1,2] [1]Department of Display Convergence Engineering, Sungkyunkwan University, [2]Department of Electrical and Computer Engineering, Sungkyunkwan University

2026년 1월 30일(금), 09:00-10:45
Room A(4층, 그랜드볼룸 I+II)

D. Thin Film Process Technology 분과

O67_[FA1-D] Advanced Thin Films and Growth Processes

좌장: 한정환 교수(서울과학기술대학교), 엄태용 교수(세종대학교)

FA1-D-1 09:00-09:15	**Atomic Layer Annealing of High-Quality Wide-Bandgap BeO for Advanced 3D IC Applications** Byung Jun Yu[1,2], Jong Hyun Bae[1,2], Dohwan Jung[1], Haekyun Bong[1,2], Jongha Lim[1,2], Siwon Lee[1,2], and Jungwoo Oh[1,2] [1]School of Integrated Technology, Yonsei University, [2]BK21 Graduate Program in Intelligent Semiconductor Technology, Yonsei University
FA1-D-2 09:15-09:30	**증착 방법에 따른 Poly-Si의 결정립 구조 및 전기적 특성 연구** 김성준[1,4], 박준형[2,4], 정회윤[2,4], 변병훈[2,4], 박인성[3], 이태호[4], 신왕철[4], 박영욱[4], 안진호[1,2,4] [1]한양대학교 나노반도체공학과, [2]한양대학교 신소재공학과, [3]한양대학교 나노과학기술연구소, [4]극한스케일·극한물성-이종집적 한계극복 반도체 기술 연구센터
FA1-D-3 09:30-09:45	**PECVD SiCO Thin Films Deposition: Compositional Control Using Hollow Cathode Plasma** Jun Seok Moon[1], So Yeong Park[2], Sang Hyun Lee[2], Dong Kyun Lee[2], and Tae Joo Park[1] [1]Department of Materials Science & Chemical Engineering, Hanyang University, [2]SK hynix Inc.
FA1-D-4 09:45-10:00	**Epitaxial Growth of Single-Phase NiCo Thin Films for Resistivity Size Effect Suppression in Advanced Interconnects** Ju Young Sung[1,2], Chae Hyun Lee[1,2], Ye Bin Lim[1,2], In Su Oh[1,2], Sang Hyeok Lee[1,2], Min Seo Kim[1,2], Yun Won Song[1,2], and Sang Woon Lee[1,2] [1]Department of Energy Systems Research, Ajou University, [2]Department of Physics, Ajou University
FA1-D-5 10:00-10:15	**Epitaxial Growth and Reduced Resistivity Size Effect of Single-Phase Body-Centered Cubic Co-Mo Alloy Thin Films** Ye Bin Lim[1,2], Ju Young Sung[1,2], Chae Hyun Lee[1,2], In Su Oh[1,2], Sang Hyeok Lee[1,2], and Sang Woon Lee[1,2] [1]Department of Energy Systems Research, Ajou University, [2]Department of Physics, Ajou University
FA1-D-6 10:15-10:30	**Carrier Concentration Control and Thermoelectric Enhancement of n-Type Bi_2Te_3-Based Materials via Atomic-Layer-Deposited In_2O_3 Interfacial Layers** Gwang Min Park[1,2], Ji Ho Jeon[3], Jaebaek Ju[1,4], Jin-Sang Kim[1], Seung-Hyub Baek[1,5], Jeong Hwan Han[3], and Seong Keun Kim[1,2] [1]Electronic and Hybrid Materials Research Center, KIST, [2]KU-KIST Graduate School of Converging Science and Technology, Korea University, [3]Department of Materials Science and Engineering, Seoul National University of Science & Technology, [4]Department of Materials Science and Engineering, Korea University, [5]Division of Nanoscience and Technology, KIST School, University of Science and Technology
FA1-D-7 10:30-10:45	**Compositional Engineering of Oxygen Contents in TiO_{2-x} to Enhance Temperature Sensitivity for High-Temperature Microbolometer Applications** Jeongeun Mo[1,2], Dongrye Choi[1], Daesan Han[1,2], Jeong Min Baik[2], Donghee Park[1], and Won Jun Choi[1] [1]KIST, [2]Sungkyunkwan University

2026년 1월 30일(금), 09:00-10:30
Room B(4층, 그랜드볼룸 III)

B. Patterning (Lithography & Etch Technology) 분과

O68_[FB1-B] Wet & Dry Etch Processes

좌장: 이원준 교수(세종대학교), 채희엽 교수(성균관대학교)

초청발표 **FB1-B-1** 09:00-09:30	**Advances in Atomic Layer Surface Preparation for Next-Generation Memory Nodes** Gyu Hyun Kim SK hynix University, SK hynix
FB1-B-2 09:30-09:45	**결정 방향성 기반 습식 식각을 통한 다층 WSe_2의 전하 수송 이방성 규명** 김정민, 김지현 서울대학교 화학생물공학부
FB1-B-3 09:45-10:00	**Isotropic Atomic Layer Etching of Amorphous and Crystalline Hafnium Oxide Films Using NF_3 Remote Plasma** Jehwan Hong[1], Hye-Lee Kim[1,2], Byungchul Cho[3], Changkyu Lee[3], Juhwan Park[3], and Won-Jun Lee[1,2] [1]Department of Nanotechnology and Advanced Materials Engineering, Sejong University, [2]Metal-organic Compounds Materials Research Center, Sejong University, [3]Wonik IPS
FB1-B-4 10:00-10:15	**Energy-Efficient Plasma-Assisted Atomic Layer Etching of Ruthenium via Gas Activation**ㅇ Jeongmin Oh[1], Hyung-Gu Kang[2], Gunsu Yun[2], and Jihwan An[1] [1]Graduate School of Semiconductor Technology, POSTECH, [2]Division of Advanced Nuclear Engineering, POSTECH
FB1-B-5 10:15-10:30	**Acetic Acid-Assisted Plasma-Enhanced Atomic Layer Etching for Redeposition-Free Anisotropic Cobalt Profiles** Harin Song[1,2], Daehan Won[1,2], Dahui Jeon[1,2], Hongju Yang[1,2], Chee Won Chung[1,2], and In-Hwan Baek[1,2] [1]Department of Chemical Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University

2026년 1월 30일(금), 09:00-10:45
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O69_[FC1-D] Atomic Layer Deposition I

좌장: 송봉근 교수(홍익대학교), 오일권 교수(아주대학교)

FC1-D-1 09:00-09:15	**Initial Growth Study of Pt Atomic Layer Deposition for Continuous and Low-Resistivity Ultrathin Films** Seon Gu Choi, Eun Ji Joo, Jeong Min Han, Jae Hyeon Lee, and Jeong Hwan Han Department of Materials Science and Engineering, Seoul National University of Science & Technology
FC1-D-2 09:15-09:30	**Theoretical Analysis of Temperature-Dependent Behavior in Area-Selective Atomic Layer Deposition of Ruthenium Using a Novel Precursor** Iaan Cho[1,2], Hideaki Nakatsubo[3,4], Jeongha Kim[3], Hyungjun Kim[2], Soo-Hyun Kim[3], and Bonggeun Shong[1] [1]Hongik University, [2]Yonsei University, [3]UNIST, [4]Tanaka Precious Metal Technologies Co., Ltd.
FC1-D-3 09:30-09:45	**Theoretical Insights into Factors Determining Deposition Selectivity During Area-Selective ALD of Ru Using Small-Molecule Inhibitors** Myeong Kyun Nam[1], Jiwon Kim[1], Iaan Cho[1,2], Young Min Lee[3], Gi-Young Jo[3], Jeong Yub Lee[3], Eun-Hyoung Cho[3], and Bonggeun Shong[1] [1]Hongik University, [2]Yonsei University, [3]Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd.
FC1-D-4 09:45-10:00	**Metal-on-Metal Area-Selective Atomic Layer Deposition of Ruthenium with Infinite Selectivity for Advanced BEOL Interconnects** Dahui Jeon[1,2], Tien Anh Nguyen[3], Sieun Chae[3], and In-Hwan Baek[1,2] [1]Department of Chemical Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University, [3]School of Electrical Engineering and Computer Science, Oregon State University
FC1-D-5 10:00-10:15	**Advanced Atomic Layer Deposition: Titanium Nitride Thin Films Growth Using Discrete Feeding Method with Brute Hydrazine** Jae Woo Jang, Ji Won Han, In Chan Jeong, and Tae Joo Park Department of Materials Science & Chemical Engineering, Hanyang University
FC1-D-6 10:15-10:30	**Alternative Reaction Pathways to Reduce the Resistivity of Low-Temperature Atomic Layer Deposition of TiN Electrode Films** Kyeong Hyeon Choi[1,2], Byeong Jun Jeon[1,2], Se Eun Kim[1,2], Kyung Jun Lee[1,2], Tae Hyun Kim[1,2], Se Eun Park[1,2], Seung Min Noh[3], Jae Min Jang[3], Bong Geun Shong[3], and Sang Woon Lee[1,2] [1]Department of Physics, Ajou University, [2]Department of Energy Systems Research, Ajou University, [3]Department of Chemical Engineering, Hongik University
FC1-D-7 10:30-10:45	**Low-Resistivity Thin Vanadium Nitride (VN) Films Using Plasma-Enhanced Atomic Layer Deposition for Advanced Cu Diffusion Barrier** Kangbaek Seo[1], Hyunjin Lim[2], Seungchae Lee[2], Youngseo Na[1], Yehbeen Im[2], Dounguk Kim[1], Hyunseok Oh[3], Donghun Shin[3], Yongjoo Park[3], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University, [3]SK Trichem Co., Ltd.

2026년 1월 30일(금), 09:00-10:30
Room D(5층, 컨벤션홀 L)

K. Memory (Design & Process Technology) 분과

O70_[FD1-K] Advanced Memory

좌장: 김시준 교수(강원대학교), 김성준 교수(동국대학교)

초청발표 **FD1-K-1** 09:00-09:30	**CMOS-compatible Gate Insulator Stack Engineering for Hardware-Based Spiking Neural Networks** Min-Kyu Park Department of Semiconductor Engineering, Gachon University
FD1-K-2 09:30-09:45	**Threshold Voltage and Saturation Current Programmable Charge-trap Oxide Transistor and Its Utilization for Time-Based Cryptography** Huisu Noh and Kyung Min Kim Graduate School of Semiconductor Technology, KAIST
FD1-K-3 09:45-10:00	**Enhanced Polarization Switching in InGaAs MFIS Tunnel FET** Kyul Ko, Dae-Hwan Ahn, and Jae-Hoon Han KIST
FD1-K-4 10:00-10:15	**Carbon-Doped GST PCRAM: Correlating Chemical Bonding with Thermal Stability and Retention** Jisu Park[1], Seung Min Kang[1], Woo Seong Son[1], and Changhwan Choi[1,2] [1]Department of Semiconductor Engineering, Hanyang University, [2]Division of Materials Science and Engineering, Hanyang University
FD1-K-5 10:15-10:30	**Sidewall-Structured Memristor for High Density Arrays** Sooyeon Narie Kay, Dong Hwi Hwang, and Kyung Min Kim Department of Materials Science and Engineering, KAIST

2026년 1월 30일(금), 09:00-10:45
Room E(5층, 에메랄드)

J. Nano-Science & Technology 분과

O71_[FE1-J] 3D 집적·회로 기술 및 나노소자

좌장: 조경준 선임(KIST), 최상현 교수(DGIST)

초청발표 **FE1-J-1** 09:00-09:30	**Improving Transistor Performance through New Material Research** Yongsung Kim, Kyung-Eun Byun, Minsu Seol, Eun-Kyu Lee, Changhyun Kim, Min Seok Yoo, Junyoung Kwon, Huije Ryu, Sang Won Kim, and Luhing Hu Device Research Center, Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd.
초청발표 **FE1-J-2** 09:30-10:00	**Radiation-Hardened Electronics based on Low-Dimensional Materials** Yeonhoo Kim KRISS
FE1-J-3 10:00-10:15	**Modular Approach for Monolithic 3D Integration of CFETs through Inter-module Vias** Hyokwang Park[1,2], Won Jong Yoo[1,2], and Boseok Kang[1,2,3,4] [1]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University, [2]Department of Nano Science and Technology, Sungkyunkwan University, [3]Department of Nano Engineering, Sungkyunkwan University, [4]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
FE1-J-4 10:15-10:30	**CMOS-Integrable Ambipolar Tellurene Nanofilm-Based Negative Differential Transconductance Transistor for Multi-Valued Logic Computing** Jihoon Huh[1,2], Bolim You[1,2], Yuna Kim[1], Mino Yang[3], Unjeong Kim[4], Min-Kyu Joo[5,6], Myung Gwan Hahm[1,7], and Moonsang Lee[1,2] [1]Inha University, [2]Program in Semiconductor Convergence, Inha University, [3]KBSI, [4]Department of Physics, Dongguk University, [5]Department of Applied Physics, Sookmyung Women's University, [6]Institute of Advanced Materials and Systems, Sookmyung Women's University, [7]Institute for Bio-Medical and Translational Health Care, Inha University Hospital
FE1-J-5 10:30-10:45	**EMI Shielding Through Engineering 2D Materials Based Nanomatrix** Jong Sung Kim[1,2], Eunjung Lee[1,3], and Kyungjune Cho[2] [1]Convergence Research Center for Solutions to Electromagnetic Interference in Future-mobility, KIST, [2]Department of Materials Science and Engineering, Korea University, [3]Department of Chemical and Biological Engineering, Korea University

2026년 1월 30일(금), 09:00-10:45
Room F(5층, 사파이어)

K. Memory (Design & Process Technology) 분과

O72_[FF1-K] Advanced Memory

좌장: 권민우 교수(서울과학기술대학교), 권동석 교수(GIST)

FF1-K-1 09:00-09:15	**Low-Frequency Noise Characteristics of Hafnia Ferroelectric FETs with Ultra-Thin Interface Layer** Youngchan Cho[1], Changhyeon Han[2], Daewoong Kwon[2], and Wonjun Shin[1] [1]Department of Semiconductor Convergence Engineering, Sungkyunkwan University, [2]Department of Electrical Engineering, Hanyang Unversity
FF1-K-2 09:15-09:30	**A Tripartite Synapse-Inspired Ferroelectric-Gated Phototransistors for In-Sensor Image Processing** Yubin Lee[1], Dong Hyun Seo[1], June Seo Lee[2], Jae Min Jeon[2], and Young Min Song[1] [1]School of Electrical Engineering, KAIST, [2]School of Electrical Engineering and Computer Science, GIST
FF1-K-3 09:30-09:45	**Variation Tolerant Probabilistic Computing Using a Probabilistic Von Neumann (p-VN) Extraction Algorithm** Seoeun Jang and Kyung Min Kim KAIST
FF1-K-4 09:45-10:00	**Reconfigurable Mott Oscillators for Hardware Security and Computing** Daehee Kim[1], Gwangmin Kim[2], and Kyung Min Kim[1] [1]Department of Materials Science and Engineering, KAIST, [2]Peter-Grünberg-Institut 7 (PGI-7), Forschungszentrum Jülich GmbH
FF1-K-5 10:00-10:15	**Hardware Security Enhancement via Self-Differential Pair PUF in 3D-Stacked Memristor Crossbar Array** Jinwoo Park and Hyungjin Kim Division of Materials Science and Engineering, Hanyang University
FF1-K-6 10:15-10:30	**Variation Tolerant Co-Design of Selector-Memory Pairs for Cross-Point Array** Moon Gyu Choi, Su Yong Chae, and Seung Hwan Lee Department of Semiconductor Engineering, Kyung Hee University
FF1-K-7 10:30-10:45	**Physical Unclonable Function based on Wordline-Controlled String Current Variation in 3D NAND Flash for Enhanced Reliability** Dayeon Yu[1,2], Hwiho Hwang[1,2], and Hyungjin Kim[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University

2026년 1월 30일(금), 09:00-10:45
Room G(5층, 루비 II)

A. Interconnect & Package 분과

O73_[FG1-A] Advanced Package IV

좌장: 남태욱 교수(세종대학교), 김명준 교수(성균관대학교)

초청발표 **FG1-A-1** 09:00-09:30	**DIC 측정 기반 패키지 인터커넥트 열기계 변형 거동 규명** 이태익 한국생산기술연구원 첨단반도체패키징집적센터
FG1-A-2 09:30-09:45	**Effect of Substrate Thickness and Material Properties on Package Warpage Reduction** Jong Won Lee[1,2], Jae Bum Choi[1,2], and Jae Woo LEE[2] [1]Package Development, SK hynix, [2]Department of Electronics and Information Engineering, Korea University
FG1-A-3 09:45-10:00	**Projection Moiré 기술을 활용한 Advanced PKG Warpage 평가** 정두진, 김제민, 이규석 한국전자기술연구원 신뢰성연구센터
FG1-A-4 10:00-10:15	**Development of Next-generation Spiral Scan Based High-throughput Inline SAT Machine for Future HBM Core Inspection Technology** Han Nu Ri Park, Young Hoon Lee, Gwangmin Yoon, Jongwook Kwon, and Kyungmin Lee SK hynix Co., Ltd.
FG1-A-5 10:15-10:30	**Probabilistic Fracture of Glass Interposer for TGV Semiconductor Applications** 박민혁[1], 김해탄[1], 박수현[1], 김동오[1], 박창규[1], 좌성훈[1], 오정원[2], 신현록[2], 박지웅[2], 변재원[1] [1]서울과학기술대학교 신소재공학과, [2](주)제이더블유엠티
FG1-A-6 10:30-10:45	**Vacancy Assisted Metal-Oxide Redox Bonding for Low Temperature Integration** 이지윤, 성동윤, 최서연, 홍슬기 서울과학기술대학교 지능형반도체공학과

2026년 1월 30일(금), 09:00-10:45
Room H(6층, 스페이드)

G. Device & Process Modeling, Simulation and Reliability 분과

O74_[FH1-G] Device & Process Modeling, Simulation and Reliability VI

좌장: 장지원 교수(연세대학교), 최성진 교수(국민대학교)

FH1-G-1 09:00-09:15	**Analysis of Retention Characteristics Considering Floating Body Effects in Double-Gate, Gate-All-Around and Channel-All-Around MOSFETs Used as Cell Transistors for 3-Dimensional DRAM** Ga-Min Gwon and Ji-Woon Yang Department of Electronics and Information Engineering, Korea University
FH1-G-2 09:15-09:30	**Asymmetry-Based Identification of Grain-Boundary Position and Its Impact on Device Variability in 3-D NAND Flash Memory** Daehan Won[1], Donghyun Go[2], Donghwi Kim[2], Seungjae Kim[1], Hyunjun Kim[1], and Jeong-Soo Lee[1,2] [1]Graduate School of Semiconductor Technology, POSTECH, [2]Department of Electrical Engineering, POSTECH
FH1-G-3 09:30-09:45	**Short-Channel Effects Model of Double-Gate MOSFET with a-IGZO Channel for Cell Array Transistor in 3-Dimensional DRAM** Tae-Hyun Park and Ji-Woon Yang Department of Electronics and Information Engineering, Korea University
FH1-G-4 09:45-10:00	**An Approach for BSIM-CMG Parameter Extraction Using a Quasi-1D Model** Kwang-Woon Lee and Sung-Min Hong Department of Electrical Engineering and Computer Science, GIST
FH1-G-5 10:00-10:15	**Investigation of a Methodology for Adjusting the Ron of ESD Devices through Experiments** Jihoon Lee and Youngchul Kim Technology Development Department, DB HiTek
FH1-G-6 10:15-10:30	**Top-gate Self-aligned IGZO TFT의 측방향 수소 확산 매커니즘 규명 및 제어를 통한 수소 열처리 내성 향상** 김희태[1], 이호석[1], 김희수[1], 조성행[2], 조병진[1] [1]한국과학기술원 전기 및 전자공학부, [2]한국전자통신연구원 플렉시블 전자소자연구실
FH1-G-7 10:30-10:45	**Mechanism Analysis of High-Voltage ESD BJT Protection Circuit with High Current Characteristic** Bo-Bae Song and Young-chul Kim ESD/TCAD Team, DB HiTek

2026년 1월 30일(금), 09:00-10:45
Room I(6층, 하트)

Q. Metrology, Inspection, Analysis, and Yield Enhancement 분과

O75_[FI1-Q] Metrology, Inspection, Analysis, and Yield Enhancement III

좌장: 손영훈 마스터(삼성전자), 제갈원 박사(한국표준과학연구원)

초청발표 **FI1-Q-1** 09:00-09:30	**A Study on Prediction of Electrical Characteristics Using In-Line Measurement Values in GAA FET** Hyung Keun Yoo, Kyunghoon Lee, Inhee Jung, Yeonjeong Kim, Mingyu Kim, Mira Park, Younghoon Sohn, and Yongdeok Jeong Metrology & Inspection Technology Team, Common Technology Center, Samsung Electronics Co., Ltd.
초청발표 **FI1-Q-2** 09:30-10:00	**Patent Big Data Analytics of Gas and Chemical Systems for Semiconductor Infrastructure: Implications for Metrology and Process Control** Jongmin Lee Global Manufacturing & Infra Technology, Samsung Electronics Co., Ltd.
FI1-Q-3 10:00-10:15	**Improvement of CD-SEM Image Quality with High Depth of Focus (DOF) Beam** Ra Seong Ki[1], Jong Hoi Cho[1], Kyung Su Byun[1], Jin Hee Han[1], Jun Ho Lee[1], Su Jin Lim[2], Woo Sung Jung[2], and Eun Hyuk Choi[1] [1]SK hynix Inc., [2]PDC Business Group, Applied Materials, Inc.
FI1-Q-4 10:15-10:30	**HBM Hybrid Bonding향 CMP 공정 품질 모니터링 고속화 기술 연구 (High Speed CMP Process Quality Monitoring Technology for HBM Hybrid Bonding Process)** 박품성, 조한샘, 조선기, 변정훈, 김종관 SK hynix Inc. ADV PKG MI개발
FI1-Q-5 10:30-10:45	**Anomaly Monitoring Framework Using AI-Based Chart Image Classifier and Initial Analysis Assistant** Bumsuk Chung, Jinsik Kim, Haeyong Joung, Sungjoon Hong, Yunhee Kim, Hyunjin Wang, Hyunsoo Kim, Taehwa Oh, Inkap Chang, and Chiyong An Memory Quality & Reliability, Memory Business, Samsung Electronics Co., Ltd

2026년 1월 30일(금), 09:00-10:45
Room J(6층, 다이아몬드)

I. MEMS & Sensors Systems 분과

O76_[FJ1-I] MEMS and Sensor System III

좌장: 박윤석 교수(경희대학교), 윤홍준 교수(가천대학교)

초청발표 **FJ1-I-1** 09:00-09:30	**Closed-loop Functionalities in Optical Materials and Devices** Sang Min Won Department of Electrical and Computer Engineering, Sungkyunkwan University
FJ1-I-2 09:30-09:45	**Orientation-Tunable Liquid-Crystalline Organic Semiconductors for Reconfigurable PUF and OFET Applications** Moon Jong Han Department of Semiconductor Engineering, Gachon University
FJ1-I-3 09:45-10:00	**Synaptic Nanowire Phototransistor for Biosignal Classification** Wangmyung Choi[1], Jin Seok Yoon[2], Won Woo Lee[3], Gun Ho Hong[4], Hyeonjung Kim[4], Seyong Oh[4], Young Tea Chun[2], and Hocheon Yoo[1] [1]Department of Electronic Engineering, Hanyang University, [2]Division of Electronics and Electrical Information Engineering, Korea Maritime & Ocean University, [3]Department of Artificial Intelligence Semiconductor Engineering, Hanyang University, [4]Division of Electrical Engineering, Hanyang University ERICA
FJ1-I-4 10:00-10:15	**LSPR-Driven Photodetector Enabled by Ag Mesh-Si Schottky Nanodiodes** Jongyeol Park[1,2], Jihoon Huh[1,2], Yohan Lee[1,2], Seung Ji Lo[1,2], Jae Hyun Kim[1,2], Narea Lee[1,2], Jeahyeong Park[1], and Moonsang Lee[1,2] [1]Department of Materials Science and Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University
FJ1-I-5 10:15-10:30	**On-Chip Gas Leak Source Estimation Using Filament Events** Wooseong Roh[1,2], Hunhee Shin[1,2], Jonghyun Ko[1,2], Jeseung Jeong[1,2], Jong-Ho Lee[1,2], and Gyuweon Jung[1,2,3] [1]Department of Electrical and Computer Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University, [3]School of Transdisciplinary Innovations, Seoul National University
FJ1-I-6 10:30-10:45	**Grain-Boundary-Driven Stochastic Oxide Junction in 2D SnSe Enables Dual Electrical-Optical PUFs** Jaechan Song[1], Taehyun Park[2], Youngmin Han[2], Junhyung Cho[1], and Hocheon Yoo[2] [1]Department of Artificial Intelligence Semiconductor Engineering, Hanyang University, [2]Department of Electronic Engineering, Hanyang University

2026년 1월 30일(금), 10:55-12:40
Room C(5층, 컨벤션홀 W)

D. Thin Film Process Technology 분과

O77_[FC2-D] Atomic Layer Deposition II

좌장: 한정환 교수(서울과학기술대학교), 유찬영 교수(홍익대학교)

FC2-D-1 10:55-11:10	**High-Temperature Atomic Layer Deposition of High-Quality SiO_2 Films Using a Novel Silylamine-Type Precursor** Okhyeon Kim[1], Changgyu Kim[1], Tanzia Chowdhury[1], Mi-Soo Kim[1], Taeyoon Kwon[1], Hye-Lee Kim[1], Seunggyun Hong[2], Byung-Kwan Kim[2], Jin Sik Kim[2], Wonyong Koh[2], and Won-Jun Lee[1] [1]Department of Nano Technology and Advanced Materials Engineering, Sejong University, [2]UP Chemical Co., Ltd.
FC2-D-2 11:10-11:25	**Oxygen Vacancy Suppression in ALD TiO_2 Thin Films Using a Modified Ti-Precursor** Juan Hong, Seokho Cho, Hyeongjun Kim, Taehyun Kim, Soonbin Kwon, and Woongkyu Lee Department of Materials Science and Engineering, Soongsil University
FC2-D-3 11:25-11:40	**Temperature-Driven Phase Formation with Novel Cyclopentadienyl-Based Precursors for BEOL-Compatible $Hf_{1-x}Zr_xO_2$ Ferroelectric Capacitors** Hye-Won Cho[1], Hyo-Bae Kim[1], Jin Sik Kim[2], Byung-Kwan Kim[2], and Ji-Hoon Ahn[1] [1]Department of Materials Science & Chemical Engineering, Hanyang University, [2]Material Process Development Division, UP Chemical Co., Ltd.
FC2-D-4 11:40-11:55	**A Composition Tuning Strategy via Analysis of Underlayer-Dependent Initial Growth Behavior in IGZO Supercycle ALD** Jae-Hak Choung[1], Ae-Rim Choi[1], Eun-Hu Hwang[1], Seung-Wook Ryu[2], and Il-Kwon Oh[1,3] [1]Department of Intelligence Semiconductor Engineering, Ajou University, [2]Revolutionary Technology Center, R&D Process, R&D Division, SK hynix Inc., [3]Department of Electrical and Computer Engineering, Ajou University
FC2-D-5 11:55-12:10	**ALD-Grown Amorphous $InGaO_x$ Channels for Thermally Stable Thin-Film Transistors** Joonyong Kim, Dong Hee Han, Hyun Woo Jeong, Hyeong Seok Choi, Jaejoon Kim, Suyong Lee, and Min Hyuk Park Department of Materials Science and Engineering, Seoul National University
FC2-D-6 12:10-12:25	**Low-Damage IGZO/HfO_2 Charge-Trap Memory Devices Fabricated by a Customized 2600W Remote Plasma ALD Process** In Kook Hwang, Ji Won Kim, Byung Wook Kim, Young Woon Jang, Hyeon Wu Nam, Min Kyun Kang, and Chang Bun Yoon Department of Advanced Materials Engineering, Tech University of Korea
FC2-D-7 12:25-12:40	**Transparent Resistive Memory Devices Utilizing Ga-Doped ZnO Thin Films Prepared by Atomic Layer Deposition** Wonnyeon Kim, Gyeongil Son, Satish B. Jadhav, and Minjae Kim School of Materials Science & Engineering, Yeungnam University

2026년 1월 30일(금), 10:55-12:40
Room D(5층, 컨벤션홀 L)

O. System LSI Design 분과

O78_[FD2-O] R & O 분과 통합 세션 (부제: System LSI Design)

좌장: 유호영 교수(충남대학교), 김재호 교수(경상국립대학교)

초청발표 **FD2-O-1** 10:55-11:25	**Device/Circuit Design for Emerging eDRAM Technologies** Munhyeon Kim Department of Electrical and Information Engineering, Seoul National University of Science and Technology
FD2-O-2 11:25-11:40	**하드웨어 효율적인 GPS L1C 인터리버 구현** 송재오, 황용택, 구교덕, 김도훈, 유호영 충남대학교 전자공학과
FD2-O-3 11:40-11:55	**A 512-Point STFT Hardware Architecture Using Low-Precision Floating-Point for High Accuracy and Area Efficiency** Seung Pyo Hong[1], Hana Kim[2], and Ji-Hoon Kim[1,2] [1]Department of Artificial Intelligence Semiconductor Engineering, Hanyang University, [2]Department of Electronic Engineering, Hanyang University
FD2-O-4 11:55-12:10	**An Efficient Multi-Mode SHA-3 Architecture** Jisoo Lee, Sojeong Ok, and Woong Choi School of Electronic Engineering, Sookmyung Women's University
FD2-O-5 12:10-12:25	**FTL 개발자를 위한 Cosmos OpenSSD 시뮬레이터 상 개발환경** 이제연, 최종무 단국대학교
FD2-O-6 12:25-12:40	**Fast and Efficient Transformer-Based Architecture for SSD Failure Prediction in Multi-Horizon Forecasting** Jobeda Khanam Ria and Jaeho Kim Department of AI Convergence Engineering, Gyeongsang National University

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Room E(5층, 에메랄드)

J. Nano-Science & Technology 분과

O79_[FE2-J] 뉴로모픽·메모리 소재 및 시냅스 소자 기술

좌장: 김연후 책임연구원(한국표준과학연구원), 정용진 교수(국립한국교통대학교)

초청발표 **FE2-J-1** 10:55-11:25	**Wafer-scale Passive Crossbar Integration of Metal-oxide Memristors for Computing** Sanghyeon Choi[1,2] [1]Department of Electrical Engineering & Computer Science, DGIST, [2]Department of Semiconductor Engineering, DGIST
FE2-J-2 11:25-11:40	**나노결정질 MoS_2/HfO_2 기반 전하 포획 시냅스 소자의 공정 변수 최적화 및 전기적 특성 분석** 이정빈[1], 황윤아[1], 명재민[2,3], 김태현[2,3], 손시훈[3], 최현빈[3], 김근석[3], 김태성[3], 문지훈[2], 최민섭[1] [1]충남대학교, [2]한국표준과학연구원, [3]성균관대학교
FE2-J-3 11:40-11:55	**Reconfigurable Artificial Multipolar Neuronal Device Realized by Nanoporous VO_2 Memristive Array** Gwanyeong Park[1], Young Ran Park[1], Mingyu Kim[1], Sanghyeon Choi[3], and Gunuk Wang[1,2] [1]KU-KIST Graduate School of Converging Science and Technology, Korea University, [2]Department of Integrated Energy Engineering, Korea University, [3]Department of Electrical Engineering & Computer Science, DGIST
FE2-J-4 11:55-12:10	**Energy-efficient Uncertainty Quantification via Gate-tunable 1A1M Synaptic Device for Bayesian Neural Network** Hyeon Bin Kim[1], Yejin Kim[1], Yeon Seo An[1], Sanghyeon Choi[3], and Gunuk Wang[1,2] [1]KU-KIST Graduate School of Converging Science and Technology, Korea University, [2]Department of Integrative Energy Engineering, Korea University, [3]Department of Electrical Engineering & Computer Science, DGIST
FE2-J-5 12:10-12:25	**Improving Synaptic Properties in Ionic Gated Transistors by Controlling Ion Migration Pathways** Woongki Lee[1], Youngkyoo Kim[2], and Kyungjune Cho[1] [1]Electronic and Hybrid Materials Research Center, KIST, [2]Department of Chemical Engineering, Kyungpook National University
FE2-J-6 12:25-12:40	**A Van der Waals Optoelectronic Synapse with Tunable Positive and Negative Post-Synaptic Current for Highly Accurate Spiking Neural Networks** Dong-Ho Kang Department of Semiconductor Engineering, GIST

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Room F(5층, 사파이어)

K. Memory (Design & Process Technology) 분과

O80_[FF2-K] Advanced Memory

좌장: 김성준 교수(동국대학교), 권용우 교수(홍익대학교)

초청발표 **FF2-K-1** 10:55-11:25	**In-Memory Computing for Solving Combinatorial Optimization Problems** Dongseok Kwon Department of Semiconductor Engineering, GIST
FF2-K-2 11:25-11:40	**1T-1MFMIS FeFET CiM Cell with Enhanced Memory Window and Long-Term Multi-Bit Retention** Simin Chen[1,2], Zewei Wang[1,2], Gijun Ju[1,2,3], Jaehoon Han[3], and Younghyun Kim[1,2] [1]Department of Photonics and Nanoelectronics, Hanyang University, [2]BK21 FOUR ERICA-ACE Center, Hanyang University, [3]KIST
FF2-K-3 11:40-11:55	**Capacitive Time-Domain Ferroelectric Content-Addressable Memory for High-Density and Highly Robust In-Memory Nearest Neighbor Search** Minjeong Ryu[1,2], Jae Seung Woo[1,2], and Woo Young Choi[1,2] [1]Department of Electrical and Computer Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University
FF2-K-4 11:55-12:10	**Reliable 28nm eFlash Process for UWB-Based Automotive Applications** Gyuhak Choi, Hyunik Park, Han-Hyeoung Choi, Junyoung Kim, Taemin Jang, Jeadong Jung, Kyungjun Oh, Sooyeoung Kim, Sumin Choi, Jongyeoun Hong, Juyeong Pyo, Youngcheon Jeong, Changmin Jeon, and OhKyum Kwon Foundry Business, Samsung Electronics Co., Ltd.
FF2-K-5 12:10-12:25	**3D Integrated Neural Networks with Ionic-Switch Neurons for Energy- and Area-Efficient Hardware Implementation** Yuna Kim[1], Minsu Kang[1], Sion Kim[1], Sarah Yoon[2], Eungcheol Kim[2], Songye Lim[2], and Daeseok Lee[2] [1]School of Semiconductor Systems Engineering, Kwangwoon University, [2]Department of Electronic Materials Engineering, Kwangwoon University
FF2-K-6 12:25-12:40	**Implementation of a Leaky Integrate-and-Fire Neuron Using Volatile Memristors with Threshold Switching** Dae Kyu Lee[1,2], Gichang Noh[1], Yooyeon Jo[1,3], Eunpyo Park[1,2], Min Jee Kim[1], Heerak Wi[4], Ria Choi[4], Hyun Jae Jang[1], Suyoun Lee[1], Sangbum Kim[2], and Joon Young Kwak[4] [1]KIST, [2]Seoul National University, [3]Sun Moon University, [4]Ewha Womans University
FF2-K-7 12:40-12:55	**Polymer Insertion Effects on Self-Rectification Behaviors in CuI-RRAMs** Hyun Kyu Lee[1], Dhananjay Mishura[1], Hyeon Bin Jo[1], Yun Sung Lee[2], Han Min Kim[2], and Sung Hun Jin[1] [1]Department of Information Display, Kyung Hee University, [2]Department of Intelligent Semiconductor Engineering, Incheon National University

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Room G(5층, 루비 II)

A. Interconnect & Package 분과

O81_[FG2-A] Emerging Interconnects

좌장: 이소연 교수(인하대학교), 김명준 교수(성균관대학교)

초청발표 **FG2-A-1** 10:55-11:25	**Thermal Atomic Layer Etching of Molybdenum for the Next Generation Interconnect** Taewook Nam[1,2] [1]Department of Semiconductor Systems Engineering, Sejong University, [2]Department of Artificial Intelligence and Information Technology, Sejong University
FG2-A-2 11:25-11:40	**A Distribution-Dependent Grain Size Measurement for the Accurate Property Prediction of Ruthenium Interconnects** Jun Hyeok Hyun[1,2], Yoon-Gu Lee[3], Hongik Kim[3], Jaehee Sohn[3], Jae-Min Lim[3], Da-Young Lee[3], So-Yeon Lee[1,2], and Young-Chang Joo[3] [1]Department of Materials Science and Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University, [3]Department of Materials Science and Engineering, Seoul National University
FG2-A-3 11:40-11:55	**Plasma-Enhanced Atomic Layer Deposition of Molybdenum Carbide (MoC_x) Thin Films Using an Amido-Imido Based Metal-Organic Precursor for Conductive Interconnects** Hyunjin Lim[1], Seungchae Lee[1], Yehbeen Im[2], Youngseo Na[2], Donguk Kim[2], Kangbaek Seo[2], Kanghyeok Lee[2], Sangtae Park[1], Yong Joo Park[3], Dong Hun Shin[3], and Changhwan Choi[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University, [3]SK Trichem Co., Ltd.
FG2-A-4 11:55-12:10	**Reliability Evaluation of Cobalt Nitride (CoN) Diffusion Barrier for Advanced Cu and Co Interconnects** Yeh Been Im[1], Young Seo Na[2], Hyun Jin Lim[1], Jeng A Heo[3], So Yeon Lee[3], and Changhwan Choi[1,2] [1]Division of Materials Science and Engineering, Hanyang University, [2]Department of Semiconductor Engineering, Hanyang University, [3]Department of Materials Science and Engineering, Inha University
FG2-A-5 12:10-12:25	**Annealing Effect on the Interfacial and Dielectric Reliability of ALD Ru/ZnO Thin Films for Advanced Interconnects** Daeyoon Jeong[1], Suyeon Lee[1], Yeseul Son[2], Minwoo Kim[2], Soo-Hyun Kim[2,3], and Young-Bae Park[1] [1]School of Materials Science and Engineering, Gyeongkuk National University, [2]Graduate School of Semiconductor Materials and Devices Engineering, UNIST, [3]Department of Materials Science and Engineering, UNIST
FG2-A-6 12:25-12:40	**Benchmarking of Ag-Cu Amorphous Alloy for Interconnects Materials** SeongYun Hong[1], Subeen Lim[2], and YeongHun Lee[2] [1]Department of Intelligent Semiconductor Engineering, Incheon National University, [2]Department of Electronics Engineering, Incheon National University

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Room I(6층, 하트)

V. Quantum Technology 분과

O82_[FI2-V] Quantum Technology II

좌장: 문기원 박사(ETRI), 이문주 교수(POSTECH)

초청발표 **FI2-V-1** 10:55-11:25	**Squeezed Light Generation Using Optical Parametric Amplifier Module** Kiwon Moon, Byungkyu Jeong, Tetiana Slusar, Guhwan Kim, Hong-Seok Kim, Heesung Kim, Jaegyu Park, Jin Tae Kim, Min-su Kim, and Jung Jun Ju Quantum Technology Research Division, ETRI
초청발표 **FI2-V-2** 11:25-11:55	**The Feasibility of a Silicon Quantum Dot Structure as a Sensing Unit** Hoon Ryu School of Computer Engineering, Kumoh National Institute of Technology
초청발표 **FI2-V-3** 11:55-12:25	**Superconducting Scalable Quantum Computing** 이용호 한국표준과학연구원 초전도양자컴퓨팅시스템연구단
FI2-V-4 12:25-12:40	**Realization of an Exceptional Point in a Fabry-Pérot Cavity Using a Birefringent Defect in a Supermirror** Juman Kim[1,2], Jisung Seo[1,2], and Kyungwon An[1,2] [1]Department of Physics & Astronomy, Seoul National University, [2]Institute of Applied Physics, Seoul National University

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Room J(6층, 다이아몬드)

U. Bio-Medical 분과

O83_[FJ2-U] Sensors and Circuits for Biomedical and Biochemical Applications

좌장: 송민영 교수(DGIST), 이경태 교수(DGIST)

초청발표 **FJ2-U-1** 10:55-11:25	**A High-Density, Scalable Capacitive Neural Interface System Using 2-D Code-Division Multiplexing** Woojun Choi Department of Integrated Display Engineering, Yonsei University
초청발표 **FJ2-U-2** 11:25-11:55	**Scalable and Reproducible Fabrication of Single-CNT FETs for Single-Molecule Sensing** Yoonhee Lee Division of Biomedical Technology, DGIST
FJ2-U-3 11:55-12:10	**High-Spatiotemporal-Resolution Thermoelectric Temperature Sensor Array for Photothermal Neuromodulation** Junhee Lee[1], Dongjo Yoon[2], Yoonkey Nam[2], and Hongki Kang[3] [1]Department of Electrical Engineering and Computer Science, DGIST, [2]Department of Bio and Brain Engineering, KAIST, [3]Department of Biomedical Engineering, Seoul National University College of Medicine
FJ2-U-4 12:10-12:25	**A cDNA-Mediated Regenerable RF Biosensor based on Solution-Processed MoS_2 for Selective ss-cfDNA Detection** Seungchan Lee[1], Sung Moon Park[2], Changwoo Pyo[2], and Myungsoo Kim[1,2] [1]Department of Electrical Engineering, UNIST, [2]Graduate School of Semiconductor Materials and Devices Engineering, UNIST