



Future Normal in Semiconductor

2025-02-13(목), 10:55-12:40

좌장: 추후업데이트 예정

G. Device & Process Modeling, Simulation and Reliability 분과

[TN2-G] Device Characterization & Modeling 2

<p>TN2-G-1 10:55-11:10</p>	<p>Electron Trap Distribution in Al₂O₃/Si₃N₄ Gate Insulator Structures Joonhyung Cho^{1,2}, Joon-Hwang¹, Min-Kyu Park¹, and Jong-Ho Lee¹ ¹Department of Electrical and Computer Engineering, Seoul National University, ²Research and Development Division, SK hynix</p>
<p>TN2-G-2 11:10-11:25</p>	<p>Energy Gap and Orbital Mixing in DNNT/PTCDI-C8 Heterostructure Yeo Eun Kim, Hocheon Yoo Gachon University</p>
<p>TN2-G-3 11:25-11:40</p>	<p>Investigating Charge Transport and Recombination Dynamics in OLEDs Through Transient Electroluminescence Analysis Al Amin^{1,2} and Jeong-Hwan Lee^{1,2,3} ¹Department of Materials Science and Engineering, Inha University, ²Program in Semiconductor Convergence, Inha University, ³3D Convergence Center, Inha University</p>
<p>TN2-G-4 11:40-11:55</p>	<p>Exploring the Effect of Continuous-Wave Laser Annealing on Patterned Si Wafer with Reflectors for Selective Annealing Gunryeol Cho, Sanguk Lee, Minchan Kim, Jongseo Park, Bohyun Kang, Jaeseong Pyo, Seunghwan Lee, Junjong Lee, Yonghwan Ahn, and Rock-Hyun Baek Department of Electrical Engineering, POSTECH</p>
<p>TN2-G-5 11:55-12:10</p>	<p>Impact of Non-ideal Characteristics of SiO_x Threshold Switching Probabilistic Bits on Solving Complex Optimization Problems Jihyun Kim¹, Hyeonsik Choi², and Jiyong Woo^{1,2} ¹School of Electronics Engineering, Kyungpook National University, ²School of Electronic and Electrical Engineering, Kyungpook National University</p>
<p>TN2-G-6 12:10-12:25</p>	<p>Extraction and analysis on source resistance in In_{0.8}Ga_{0.2}As QW HEMTs considering ballistic transport Se-Hun Kim, Mun-Ho Kim, Min-Kyu Song, Seung-Woo Son, Su-Min Choi, Min-Seo Yu, In-Geun Lee, Jae-Hak Lee, and Dae-Hyun Kim School of Electronic and Electrical Engineering, Kyungpook National University</p>



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TN2-G-7
12:25-12:40

Saturation Current Ratio Method for Extraction of Parasitic Resistances with Dual Configurations in Individual MISFETs

Ji Won Park¹, Seonghyeon Jeong¹, Seung Hyeop Han¹, Hanbin Lee¹, Gyeongsu Min¹, Hyo-In Yang¹, So-Jeong Park¹, Jun-Ho Jang¹, Jeong Yeon Im¹, Dae Hwan Kim¹, Jong-Ho Bae¹, Dong Myong Kim², and Sung-Jin Choi¹

¹School of Electrical Engineering, Kookmin University, ²Department of Advanced Technology, DGIST