



# 제 32회 한국반도체학술대회

The 32nd Korean Conference on Semiconductors

2025년 2월 12일(수)-14일(금) | 강원도 하이원리조트

## *Future Normal in Semiconductor*

2025년 2월 13일(목), 15:50-17:20

Room E(에메랄드 II+III), 5층

S. Chip Design Contes 분과

### 031\_[TE3-S] Chip Design Contest

좌장:

TE3-S-1	<b>A Multi-Output Hybrid Charger for Fast Battery Charging System</b> Chanjung Park, Seongil Yeo, Geuntae Park, and Kunhee Cho Kyungpook National University
TE3-S-2	<b>A High-Resolution Linear-Exponential Incremental ADC</b> Minkyu Yang, Changjoo Park, Joeun Kim, Jeongmyeong Kim, Dalta Imam Maulana, and Wanyeong Jung KAIST
TE3-S-3	
TE3-S-4	<b>A Sub-50-fs RMS Jitter, 103.5-GHz Fundamental-Sampling PLL With an Extended Loop Bandwidth</b> Joeun Bang <sup>1</sup> , Jaeho Kim <sup>2</sup> , Seohee Jung <sup>2</sup> , and Jaehyook Choi <sup>2</sup> <sup>1</sup> KAIST, <sup>2</sup> Seoul National University