2025년 2월 13일(목), 15:50-17:20
Room E(에메랄드 II+III), 5층

S. Chip Design Contes 분과

O31_[TE3-S] Chip Design Contest

좌장:

TE3-S-1	A Multi-Output Hybrid Charger for Fast Battery Charging System Chanjung Park, Seongil Yeo, Geuntae Park, and Kunhee Cho Kyungpook National University
TE3-S-2	A High-Resolution Linear-Exponential Incremental ADC Minkyu Yang, Changjoo Park, Jooeun Kim, Jeongmyeong Kim, Dalta Imam Maulana, and Wanyeong Jung KAIST
TE3-S-3	
TE3-S-4	A Sub-50-fs RMS Jitter, 103.5-GHz Fundamental-Sampling PLL With an Extended Loop Bandwidth Jooeun Bang[1], Jaeho Kim[2], Seohee Jung[2], and Jaehyouk Choi[2] [1]KAIST, [2]Seoul National University