2025-02-13(목), 09:00-10:45
좌장: 추후업데이트 예정

K. Memory (Design & Process Technology) 분과

[TB1-K] Charge Trapped Memory Application - I

초청 TB1-K-1 09:00-09:30	**Key Challenges of VNAND Unit Cell Design for Higher Layer Stacking** Doo Hee Hwang, Sang Hoon Kim, Seung Jae Baik, and Jae duk Lee Flash TD Team, Semiconductor R&D Center, Samsung Electronics
TB1-K-2 09:30-09:45	**Array-level NAND Cell Simulator for Feasibility Assessment of Novel Memory Cells in 3D NAND Architecture** Seong Hwan Kong and Wonbo Shim Seoul National University of Science and Technology
TB1-K-3 09:45-10:00	**Improved Memory Characteristics of MONOS Device with High-k dots Embedded Si_3N_4 Charge Trap Layer** Seongho Lee[1], San Park[1], Sehyeon Choi[1], Yun Seo Lim[1], Changhwan Choi[1], Hyungjun Kim[2], Jaehyun Yang[2], Bio Kim[2], Youngseon Son[2], and Hanmei Choi[2] [1]Division of Materials Science & Engineering, Hanyang University, [2]Memory Process Development Team, Samsung Electronics
TB1-K-4 10:00-10:15	**Analysis of The Dominant Mechanism in Hybrid NAND Flash for Enhanced Memory Window** Jaeseon Eo[1], Kihoon Nam[1], Donghyun Kim[1], Jiyoon Kim[1], Rock-Hyun Baek[1], and Sanghun Jeon[2] [1]Department of Electrical Engineering, POSTECH, [2]School of Electrical Engineering, KAIST
TB1-K-5 10:15-10:30	**Leveraging Negative Capacitance for Reducing Operating Voltage in High-Density 3D NAND Technology** Sangho Lee, Yunseok Nam, Giuk Kim, Hunbeom Shin, Seokjoong Shin, and Sanghun Jeon School of Electrical Engineering, KAIST
TB1-K-6 10:30-10:45	**Unveiling the Origin of Disturbance in FeFET and the Potential of Multifunctional TiO_2 as a Breakthrough for Disturb-free 3D NAND Cell** Hyunjun Kang, Giuk Kim, and Sanghun Jeon School of Electrical Engineering, KAIST