2025-02-13(목), 09:00-10:45
좌장: 추후업데이트 예정

K. Memory (Design & Process Technology) 분과

[TA1-K] DRAM Application

초청 TA1-K-1 09:00-09:30	조현보 대표 (알세미)
TA1-K-2 09:30-09:45	Development of an Automated DTCO Methodology for Optimized DRAM Sense Amplifier Design Sueyeon Kim[1], Jaeweon Kang[2], and Jongwook Jeon[1] [1]Department of Electrical and Computer Engineering, Sungkyunkwan University, [2]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
TA1-K-3 09:45-10:00	Overcoming Leakage Challenges in Vertical Gate-all Around Architectures : A Pathway to High-Performance 3D DRAM Seong Hun Yoon[1], Jae Hyun Park[2], Jung Ho Lee[2], and Jae Kyeong Jeong[1,2] [1]Department of Display Science and Engineering, Hanyang University, [2] Department of Artificial Intelligence Semiconductor Engineering, Hanyang University
TA1-K-4 10:00-10:15	Understanding the Abnormal Capacitance of Ferroelectric HZO near Morphotropic Phase Boundary: Excellent Candidate for DRAM and Capacitive Memory Array with Non-destructive Read Operation M. Habibi[1], A. Kashir[2], S. Oh, H. Jang, and H. Hwang [1]POSTECH, [2]Ferroelectric Memory GmbH
TA1-K-5 10:15-10:30	Simulation of Capacitorless Dynamic Random-Access Memory based on GAA JLFET with Vertically Stacked Storage Layer and Underlapped Gate Structure Won Suk Koh, Sang Ho Lee, Jin Park, Min Seok Kim, Seung Ji Bae, Jeong Woo Hong, Gang San Yun, and In Man Kang School of Electronic and Electrical Engineering, Kyungpook National University
TA1-K-6 10:30-10:45	A Study on the Cb/Cs Ratio in 3.5F^2 DRAM Cell Array Hyeok Je Jeong[1], Kwang Ryeol Kim[1], Chai Rok Lim[1], Yong Soo Kim[2], Dae Young Kim[3], Jae Hyun Lee[4], and Gi Yeol Yun[1] [1]Taesung Environmental Research Institute, [2]University of Ulsan, [3]Osan University, [4]Pusan National University