



## *Future Normal in Semiconductor*

2025-02-14(금), 10:55-12:40

좌장: 추후업데이트 예정

### K. Memory (Design & Process Technology) 분과

#### [FK2-K] Ferroelectric and Oxide Channel based Memory Technology

<p>FK2-K-1 10:55-11:10</p>	<p><b>Application-Dependent Bias Scheme Optimization for Ferroelectric-Tunnel-FET-Based One-Transistor Ternary Content-Addressable Memory</b></p> <p>Minjeong Ryu, Jae Seung Woo, Yeonwoo Kim, and Woo Young Choi Department Electrical and Computer Engineering, Inter-university Semiconductor Research Center, Seoul National University</p>
<p>FK2-K-2 11:10-11:25</p>	<p><b>Achieving Low-Voltage Operation of 1T-nC FRAM via Precise Engineering of Polarization Switching Kinetics in Hafnia Ferroelectrics</b></p> <p>Sangho Lee, Giuk Kim, Chaeheon Kim, Yunseok Nam, Junghyeon Hwang, Hunbeom Shin, Seokjoong Shin, and Sanghun Jeon School of Electrical Engineering, KAIST</p>
<p>FK2-K-3 11:25-11:40</p>	<p><b>The Opportunity Of Anti-Ferroelectrics In FeFET For The Emerging Non-Volatile Memory Applications</b></p> <p>School of Electrical Engineering, KAIST</p>
<p>FK2-K-4 11:40-11:55</p>	<p><b>Comparison of Bi-Layer and Tri-Layer Structures in ZrO<sub>2</sub>/ZnO/HfO<sub>2</sub> Synaptic Devices for Improved Neuromorphic Performance</b></p> <p>Dong-Min Kim<sup>1</sup>, Yu-Bin Kim<sup>1</sup>, Sung-Ho Kim<sup>1</sup>, Chae-Min Yeom<sup>1</sup>, Shivam Kumar Gautam<sup>1</sup>, Hyuk-Min Kwon<sup>2</sup>, Yong-Goo Kim<sup>3</sup>, and Hi-Deok Lee<sup>1</sup> <sup>1</sup>Department of Electronics Engineering, Chungnam National University, <sup>2</sup>School of Electronic &amp; Electrical Engineering, Hankyong National university, <sup>3</sup>Department of Green Semiconductor System, Korea Polytechnics</p>
<p>FK2-K-5 11:55-12:10</p>	<p><b>Study of IGZO-based CTF Memory with State Updates in Array</b></p> <p>Ria Choi<sup>1</sup>, Eunpyo Park<sup>2</sup>, Heerak Wi<sup>1</sup>, Dae Kyu Lee<sup>2</sup>, Min Jee Kim<sup>2</sup>, and Joon Young Kwak<sup>1</sup> <sup>1</sup>Ewha Womans University, <sup>2</sup>KIST</p>



# 제 32회 한국반도체학술대회

The 32nd Korean Conference on Semiconductors

2025년 2월 12일(수)-14일(금) | 강원도 하이원리조트

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<p>FK2-K-6 12:10-12:25</p>	<p><b>Electrically Erasable Oxide-Semiconductor-Channel Charge Trap Flash Memory with Unipolar Operation</b> Chanyeong Go<sup>1</sup>, Seongmin Park<sup>1</sup>, and Yoonyoung Chung<sup>1,2,3</sup> <sup>1</sup>Department of Electrical Engineering, POSTECH, <sup>2</sup>Department of Semiconductor Engineering, POSTECH, <sup>3</sup>Center for Semiconductor Technology, POSTECH</p>
<p>FK2-K-7 12:25-12:40</p>	<p><b>TCAD Simulation of 6T1C IGZO-Based Synaptic Device</b> Taegyeong Oh and Sung-Min Hong School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology</p>