2025-02-14(금), 10:55-12:40
좌장: 추후업데이트 예정

K. Memory (Design & Process Technology) 분과

[FJ2-K] Oxide Channel based Memory Technology

FJ2-K-1 10:55-11:10	**Photoprogrammable OFET Memory Devices based on IGZO Floating Gate** Gyeongho Lee[1,2], Dong Hyun Lee[3], and Hocheon Yoo[3,4] [1]Department of Semiconductor Total Solution Center, KICET, [2]Department of Materials Science and Engineering, Korea University, [3]Department of Electronic Engineering, Gachon University, [4]Department of Semiconductor Engineering, Gachon University
FJ2-K-2 11:10-11:25	**Oxide Channel-Based Ferroelectric NAND Device with Enhanced Memory Window Using a Source-Tied Metal Cover Structure** Hongrae Joh, Giuk Kim, Jihye Ock, Seungyeob Kim, Sangmok Lee, Sangho Lee, and Sanghun Jeon[1] School of Electrical Engineering, KAIST
FJ2-K-3 11:25-11:40	**Comparative Evaluation of the Impact of WL Off Voltage on BL Disturbance in SOI and IGZO Cell Transistors for 4F2 DRAM Application** Seong Hoon Jeon, Wonjung Kim, Seungki Kim, Soohong Eo, Sae Him Jung, Jong-Ho Bae, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim School of Electrical Engineering, Kookmin University
FJ2-K-4 11:40-11:55	**Demonstration of Amorphous InGaZnOx 2T-DRAM Array andAnalog Operation Capability for Processing-In-Memory Application** Hyunwook Jeong[1], Junseong Park[1], Haesung Kim[1], Hyojin Yang[1], Yubin Choi[1], Hwan Jin Kim[1], Sujong Kim[1], Sung-Jin Choi[1], Dae Hwan Kim[1], Dong Myong Kim[2], Seongjae Cho[3], and Jong-Ho Bae[1] [1]School of the Electronic Engineering, Kookmin University, [2]Department of Advanced Technology, DGIST, [3]Department of Electronic and Electrical Engineering, Ewha Womans University

FJ2-K-5 11:55-12:10	**Comparative Optimization of Synaptic Characteristics in IGZO-based Memristors through Interface Engineering with Metal Electrode** Jae Woo Lee, Dong Hyeop Shin, Wonjung Kim, Seung Joo Myoung, Changwook Kim, Jong-Ho Bae, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim School of Electrical Engineering, Kookmin University
FJ2-K-6 12:10-12:25	**Highly Linear and Symmetric Multilevel IGZO 2T Synaptic Device Utilizing Identical Potentiation and Depression Pulses** Suwon Seong[1], Taejun Ha[1], and Yoonyoung Chung[1, 2, 3] [1]Department of Electrical Engineering, [2]Department of Semiconductor Engineering, [3]Center for Semiconductor Technology Convergence, POSTECH
FJ2-K-7 12:25-12:40	**Disturbance-Free Parallel Programming for Multilevel IGZO 2T Synapse** Taejun Ha[1], Suwon Seong[1], and Yoonyoung Chung[1,2,3] [1]Department of Electrical Engineering, [2]Department of Semiconductor Engineering, [3]Center for Semiconductor Technology Convergence, POSTECH