



Future Normal in Semiconductor

2025-02-14(금), 09:00-10:45

좌장: 추후업데이트 예정

G. Device & Process Modeling, Simulation and Reliability 분과

[FJ1-G] Compact Modeling

<p>FJ1-G-1 09:00-09:15</p>	<p>Vertical Channel IGZO-TFT Model for Neuromorphic Application Hyoungsoo Kim¹, Daewoong Kwon², and Hyunwoo Kim ¹Department of Electrical and Electronics Engineering, Konkuk University, ²Department of Electronic Engineering, Hanyang University</p>
<p>FJ1-G-2 09:15-09:30</p>	<p>Deterministic-Precession MTJ Device Utilizing VCMA Effect Stanislav Sin and Saeroonter Oh Sungkyunkwan University</p>
<p>FJ1-G-3 09:30-09:45</p>	<p>Large Physics Model-driven SPICE Model Generation of Ultra-Low Power GAA-MOSFET for Efficient DTCO in Semiconductor Design Premkumar Vincent¹, Johyeon Kim², Gunhee Choi², Yeongwoo Nam¹, Kyungmin Kim¹, Ye Sle Cha¹, Hyunseok Whang¹, Donghyun Jin¹, Jongwook Jeon², and Hyunbo Cho¹ ¹Alsemy Inc., ²Sungkyunkwan University</p>
<p>FJ1-G-4 09:45-10:00</p>	<p>Fully Analytical SPICE-Compatible Compact I-V Model and Parameter Extraction Procedure Considering the Density of States and Transport Mechanism in Amorphous InGaZnO Thin-Film Transistors Sae Him Jung, Seung Joo Myoung, Dong Hyeop Shin, Su Han Noh, Donguk Kim, Changwook Kim, Sung-Jin Choi, Jong-Ho Bae, Dong Myong Kim, and Dae Hwan Kim School of Electrical Engineering, Kookmin University</p>
<p>FJ1-G-5 10:00-10:15</p>	<p>Short-Channel Effects Model of Channel-All-Around MOSFETs as Cell Array Transistors for 3-Dimensional DRAM Chae-Young Kim and Ji-Woon Yang Department of Electronics and Information Engineering, Korea University</p>
<p>FJ1-G-6 10:15-10:30</p>	<p>Design of a Python-SPICE Integrated Platform for FeFET-Based VMM Circuit Simulation in Neuromorphic Computing Juhwan Park¹, Jongwook Jeon¹, and Huijun Kim² ¹Department of Electrical and Computer Engineering, Sungkyunkwan University,</p>



제 32회 한국반도체학술대회

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	² Department of Semiconductor Convergence Engineering, Sungkyunkwan University
FJ1-G-7 10:30-10:45	Accelerated Device Simulation of CFET Inverter by Using Quasi-1D Model Kwang-Woon Lee and Sung-Min Hong School of Electrical Engineering and Computer Science, GIST