2025년 2월 12일(수)-14일(금) | 강원도 하이원리조트

Future Normal in Semiconductor

2025-02-14(금), 09:00-10:45

좌장: 추후업데이트 예정

F. Silicon and Group-IV Devices and Integration Technology 분과

[FH1-F] 3D GAA/CFET Technology

	Low-Temperature Fabrication of Silicon Nanowire GAAFETs with
FH1-F-1 09:00-09:15	Excimer Laser Recrystallization for M3D Integration
	Jeong Yeon Im ¹ , Hanbin Lee ¹ , Gyeongsu Min ¹ , Hyo-In Yang ¹ , So Jeong Park ¹ , Jun-
	Ho Jang ¹ , Ji Won Park ¹ , Seonghyeon Jeong ¹ , Dae Hwan Kim ¹ , Jong-Ho Bae ¹ , Dong
	Myong Kim ³ , Min-Ho Kang ² , and Sung-Jin Choi ¹
	¹ School of Electrical Engineering, Kookmin University, ² Department of Nano-process,
	NNFC, ³ Department of Advanced Technology, DGIST
FH1-F-2 09:15-09:30	Strained Ge/Si Heterogeneous 3D Sequential CFET Featuring First
	Strain Engineered Ge Top Channel
	Hyeongrak Lim ¹ , Seong Kwang Kim ¹ , Seung Woo Lee ¹ , Youngkeun Park ¹ , Jaejoong
	Jeong ¹ , Hojin Jeong ¹ , Jinha Lim ¹ , Dae-Myeong Geum ² , Jaehoon Han ³ , Younghyun
	Kim ⁴ , Jaeyong Jeong ¹ , Byung Jin Cho ¹ , and Sanghyeon Kim ¹
	¹ KAIST, ² Inha University, ³ KIST, ⁴ Hanyang University
FH1-F-3	Photoresponsive GIDL Characterization for Simultaneous Extraction of
	Donor- and Acceptor-like Interface Trap States in Vertically Stacked Si-
	NW GAA FETs
09:30-09:45	Seohyeon Park ¹ , Donghyeon Lee ¹ , Jaewook Yoo ¹ , Minah Park ¹ , Hongseung Lee ¹ ,
	Hyeonjun Song ¹ , Soyeon Kim ¹ , Seongbin Lim ¹ , Sojin Jung ¹ , Hagyoul Bae ¹ , Yang-Kyu
	Choi ² , and TaeWan Kim ³
	¹ Jeonbuk National University, ² KAIST, ³ University of Seoul
	Transient Analysis of CFET Inverter with Backside Interconnections:
FH1-F-4	Buried Power Rails, Bottom Contacts
09:45-10:00	Seung-Woo Jung and Sung-Min Hong
	School of Electrical Engineering and Computer Science, GIST
	Implementation of a Stress Calculation Module in an In-House Process
	Emulator for Monolithic CFET
FH1-F-5	Min-Seo Jang ¹ , In Ki Kim ¹ , Seung-Woo Jung ¹ , Jeong Hyeon Yun ² , Myoung Jin Lee ² ,
10:00-10:15	and Sung-Min Hong ¹
	¹ School of Electrical Engineering and Computer Science, GIST, ² Department of
	Electronic Engineering, Chonnam National University



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FH1-F-6 10:15-10:30	A Novel 3D-SRAM Architecture based on VGAA Transistors for Advanced Al and Edge Computing Applications Changwoo Han and Changhwan Shin School of Electrical Engineering, College of Engineering, Korea University
FH1-F-7 10:30-10:45	Multi-V th through Different Inner Gates Work Functions Seungjoon Jeong, Haevin Choi, and Changhwan Shin School of Electrical Engineering, Korea University