### 2025년 2월 12일(수)-14일(금) | 강원도 하이원리조트

## Future Normal in Semiconductor

2025-02-14(금), 10:55-12:40

좌장: 추후업데이트 예정

### D. Thin Film Process Technology 분과

#### [FE2-D] Thin Film Transistors - II

	A Study of CMOS Compatible Anti-Ambipolar Transistor based on
FE2-D-1 10:55-11:10	Sputtered n-Type In-Based Oxide and p-Type Metalloid Channel
	Chanwoo Jung <sup>1</sup> , Seok Hyun Hwang <sup>2</sup> , and Jae Kyeong Jeong <sup>1,2</sup>
	Department of Display Science and Engineering, Hanyang University,
	<sup>2</sup> Department of Electronic Engineering, Hanyang University,
	Effect of Device Geometry Variation on Memory Performance of 2TOC
FE2-D-2	DRAM Cells Using Double-Layered InGaZnO Active Channel Structures
11:10-11:25	Sang Han Ko, Kyung Min Kim, and Sung Min Yoon
	Department of Advanced Materials Engineering for Information and Electronics,
	Kyung Hee University
	Influence of Oxygen Content in IGZO on the Memory Window of FeTFT
FE2-D-3	He Young Kang, Seung Hee Cha, and Jae Kyeong Jeong
11:25-11:40	Department of Electronic Engineering, Hanyang University
	Department of Electronic Engineering, Flamyang Oniversity
FE2-D-4 11:40-11:55	Reduction of Contact Resistance in MoS2 Devices Using a Sb-Based
	Semimetal Contact Structure
	Ha Yeon Choi, Hye Seong Park, Joon Soo Byeon, Ju Yong Shin, Seung Ri Jeong,
	Shivam Kumar Gautam, and Hi-Deok Lee
	Department of Electronics Engineering, Chungnam National University
FE2-D-5 11:55-12:10	Enhancing Contact Properties of MoS <sub>2</sub> based FETs by Al <sub>2</sub> O <sub>3</sub> Interlayer
	Engineering via Atomic layer deposition
	Jihoon Park, Hwi Yoon, Sanghun Lee, Seonyeong Park, Inkyu Sohn, and Hyungjun
	Kim
	School of Electrical and Electronic Engineering, Yonsei University
	Atomic Layer Deposition of Semimetallic TiS <sub>2</sub> Contact Layer for Contact
	Resistance Engineering
FE2-D-6	Minu Cho <sup>1</sup> , Jeongwoo Seo <sup>1</sup> , Hwi Yoon <sup>1</sup> , Inkyu Sohn <sup>1</sup> , Jun Hyung Lim <sup>2</sup> , Yunyong
12:10-12:25	Nam <sup>2</sup> , and Hyungjun Kim <sup>1</sup>
	<sup>1</sup> School of Electrical and Electronic Engineering, Yonsei University, <sup>2</sup> Samsung Display
	Co., Ltd
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	Ternary Logic Transistors Using Multi-Stacked 2DEG Channels in
	Ultrathin Al <sub>2</sub> O <sub>3</sub> /ZnO Heterostructures
FE2-D-7	Ji Hyeon Choi <sup>1</sup> , Tae Jun Seok <sup>1</sup> , Sang June Kim <sup>1</sup> , Tae Joo Park <sup>1</sup> , Kyun Seong Dae <sup>2</sup> ,
12:25-12:40	Jae Hyuck Jang <sup>2</sup> , Deok-Yong Cho <sup>3</sup> , and Sang Woon Lee <sup>4</sup>
	<sup>1</sup> Department of Materials Science and Chemical Engineering, Hanyang University,
	<sup>2</sup> KBSI, <sup>3</sup> Jeonbuk University, <sup>4</sup> Ajou University