2025-02-14(금), 15:10-17:10
좌장: 추후업데이트 예정

A. Interconnect & Package 분과

[FD3-A] Advanced Package 2

FD3-A-1 15:10-15:25	**대기압 기화 플라스마를 이용한 웨이퍼 본딩 기술** Wonyoung Choi, Bumki Moon, Jungshin Lee, Yongjoo Lee, Byeongtak Park, Seung ho Han, Nungpyo Hong, and Kyeongbin Lim Semiconductor R&D Center, Samsung Electronics Co., Ltd.
FD3-A-2 15:25-15:40	**TEOS SiO_2 Film Deposition Optimization for Increasing Capability and securing TSV robustness of HBM** Intae Whoang, Byung Yoon Lim, Kijun Bang, and Sang Un Lee SK hynix
FD3-A-3 15:40-15:55	**Crystal Plasticity-Based Modeling of the Influence of Microstructures and Grain Boundary Junction Types on the Cu-Cu Bonding Interface** Jae-Uk Lee[1], Hyun-Dong Lee[2], Sung-Hyun Oh[3], Jihun Kim[4], Ki-Beom Kim[5], Ho-Jin Lee[6], Yeon-Su Kim[7], Gyeong-Bim Lim[8], Sarah-Eunkyung Kim[9], Hoo-Jeong Lee[10], and Eun-Ho Lee[11] [1,2,3,4,10,11]Sungkyunkwan University, [5,7]Sk Hynix, [6,8] Samsung Electronics, [9]Seoul National University of Science of Technology
FD3-A-4 15:55-16:10	**Drive Circuit for Semiconductor Die Testing and Applications** Youngwoo Yoo and Young-Joon Kim Gachon University
FD3-A-5 16:10-16:25	**An Efficient Standardized Simulation Model for Evaluation of Board Level Reliability in Semiconductor Applications** Jaehee An[1], Sangyul Ha[1], and Wan-Kyu Choi[2] [1]Department of Semiconductor Engineering, MyongJi University, [2]DRAM Module Solution, SK Hynix
FD3-A-6 16:25-16:40	**Advanced Cu/Polymer Hybrid bonding for 3D Multi-chip Stacking Process** Jihun Kim and Jong Kyoung Park Department of Semiconductor Engineering, Seoul National University of Science and Technology

FD3-A-7 16:40-16:55	Digital Design and DOE-Based Analysis for Optimal Wire Configuration in Diode Modules Na-Yeon Choi[1,2] and Sung-Uk Zhang[1,2] [1]Digital Twin Laboratory, Dong-Eui University, [2]Center for Brain Busan 21 Plus Program