2025-02-13(목), 09:00-10:45
좌장: 추후업데이트 예정

Q. Metrology, Inspection, Analysis, and Yield Enhancement 분과

[FD1-Q] Metrology, Inspection, Analysis, and Yield Enhancement I

초청 FD1-Q-1 09:00-09:30	#N/A
초청 FD1-Q-2 09:30-10:00	반도체 FEB에서의 공정 기준에 대한 고찰부제 : In Line SEM의 Application 별 필요 기준이 무엇이며 어떤 문제점이 있는지 알아보자. 양경모 하이케이엠 주식회사
초청 FD1-Q-3 10:00-10:30	Predicting Embedded Silicon-Germane(eSiGe) Defects in Foundry PMOSFET Devices Using Machine Learning Techniques Caused by Outdoor Nanoparticles Jongmin Lee[1,2], Jungtae Park[1,2], Il-Jin Kim[2], Haeun Lee[2], and Sehoon Park[2] [1]Department of Materials Science and Engineering, Yonsei University, [2]Samsung Electronics Co., Ltd.,
FD1-Q-4 10:30-10:45	A High-density Full Wafer Structure Measurement Method based on Imaging Ellipsometry for Process Uniformity Control Jinwoo Ahn[1], Hyukjoon Cho[1], Jaehyun Son[1], Changhyeong Yoon[1], Ji-Yong Shin[1], Juntaek Oh[1], Donggun Lee[1], Seunga Lim[1], Eunsoo Hwang[1], Jinsoo Lee[1], Jaewon Lee[1], Taeyong Jo[1], Jihye Lee[2], Younghoon Sohn[3], and Myungjun Lee[1] [1]Advanced Process Development Team 4, Semiconductor R&D Center, Samsung Electronics Co., Ltd, [2]DRAM Process Architecture Team, DRAM Product & Technology, Samsung Electronics Co., Ltd, [3]Metrology & Inspection Technology Team, Common Tech Center, Samsung Electronics Co., Ltd