



## Future Normal in Semiconductor

2025-02-14(금), 15:10-17:10

좌장: 추후업데이트 예정

### G. Device & Process Modeling, Simulation and Reliability 분과

#### [FB3-G] Carrier Transport & Quantum Simulation

<p>초청 FB3-G-1 15:10-15:40</p>	<p><b>Advances in Understanding Chemical Bonding in Amorphous and Crystalline Chalcogenide semiconductors</b> Tae Hoon Lee<sup>1</sup> and Stephen R. Elliott<sup>2</sup> <sup>1</sup>Kyungpook National University, <sup>2</sup>University of Oxford</p>
<p>FB3-G-2 15:40-15:55</p>	<p><b>Tackling Multi-dimensional Poisson Equations with Mixed Boundary Conditions using Variational Quantum Algorithm</b> Minjin Choi<sup>1</sup> and Hoon Ryu<sup>2</sup> <sup>1</sup>Center for Quantum Information R&amp;D, KISTI, <sup>2</sup>Department of Artificial Intelligence Engineering, Kumoh National Institute of Technology</p>
<p>FB3-G-3 15:55-16:10</p>	<p><b>First-Principles Modeling of Non-Equilibrium Behavior in Oxide Ferroelectric Tunnel Junctions</b> Kaptan Rajput, Ryong Gyu Lee, Tae Hyung Kim, Hyeonwoo Yeo, Juho Lee, and Yong-Hoon Kim School of Electrical Engineering, KAIST</p>
<p>FB3-G-4 16:10-16:25</p>	<p><b>Quantum Transport Simulation for the Nanosheet FET including Surface Roughness Scattering</b> Phil-Hun Ahn and Sung-Min Hong School of Electrical Engineering and Computer Science, GIST</p>
<p>FB3-G-5 16:25-16:40</p>	<p><b>Evaluation of the Effect of Metal Contact Geometry on S/D Junction Resistance in Si/InGaAs FinFETs Using Semi-Classical Monte Carlo Carrier Transport Simulation</b> Jae Yeon Kim<sup>1,3</sup>, Dong Hyeok Lee<sup>2</sup>, Suk Hyeong Youn<sup>2</sup>, and Jiwon Chang<sup>1,3</sup> <sup>1</sup>Department of System Semiconductor Engineering, Yonsei University, <sup>2</sup>Department of Materials Science and Engineering, Yonsei University, <sup>3</sup>BK21 Graduate Program in Intelligent Semiconductor Technology</p>
<p>FB3-G-6 16:40-16:55</p>	<p><b>Four-coupled Multi-physics Simulations of Multi-layer Ferroelectric Field Effect Transistors with Polar Topological States</b> Yangjin Jung, Seokwon Lee, and Mincheol Shin Department of Electrical Engineering, KAIST</p>



# 제 32회 한국반도체학술대회

The 32nd Korean Conference on Semiconductors

2025년 2월 12일(수)-14일(금) | 강원도 하이원리조트

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<b>FB3-G-7</b> <b>16:55-17:10</b>	<b>Extremely Low-Power Topological Transistors</b> Yosep Park <sup>1</sup> , Yungyeong Park <sup>2</sup> , Subeen Lim <sup>2</sup> , and Yeonghun Lee <sup>1,2</sup> <sup>1</sup> Department of Intelligent Semiconductor Engineering, Incheon National University, <sup>2</sup> Department of Electronics Engineering, Incheon National University
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