2025년 2월 13일(목), 10:55-12:40
Room N(다이아몬드 II), 6층

G. Device & Process Modeling, Simulation and Reliability 분과

O26_[TN2-G] Device Characterization & Modeling 2

좌장: 장지원 교수(연세대학교), 우지용 교수(경북대학교)

TN2-G-1 10:55-11:10	**Electron Trap Distribution in Al_2O_3/Si_3N_4 Gate Insulator Structures** Joonhyung Cho[1,2], Joon Hwang[1], Min Kyu Park[1], and Jong Ho Lee[1] [1]Department of Electrical and Computer Engineering Seoul National University, [2]Research and Development Division, SK Hynix Inc.
TN2-G-2 11:10-11:25	**Energy Gap and Orbital Mixing in DNTT/PTCDI-C8 Heterostructure** Yeo Eun Kim and Hocheon Yoo Gachon University
TN2-G-3 11:25-11:40	**Investigating Charge Transport and Recombination Dynamics in OLEDs through Transient Electroluminescence Analysis** Al Amin[1,2] and Jeong-Hwan Lee[1,2,3] [1]Department of Materials Science and Engineering, Inha University, [2]Program in Semiconductor Convergence, Inha University, [3]3D Convergence Center, Inha University
TN2-G-4 11:40-11:55	**Exploring the Effect of Continuous-Wave and Pulsed Laser Annealing on Patterned Si Wafer with Reflectors for Selective Annealing** Gunryeol Cho, Sanguk Lee, Minchan Kim, Jongseo Park, Bohyun Kang, Jaeseong Pyo, Seunghwan Lee, Junjong Lee, Yonghwan Ahn, and Rock-Hyun Baek Department of Electrical Engineering, POSTECH
TN2-G-5 11:55-12:10	**Impact of Non-ideal Characteristics of SiO_x Threshold Switching Probabilistic Bits on Solving Complex Optimization Problems** Jihyun Kim[1], Hyeonsik Choi[2], and Jiyong Woo[1,2] [1]School of Electronics Engineering, Kyungpook National University, [2]School of Electronic and Electrical Engineering, Kyungpook National University
TN2-G-6 12:10-12:25	**Extraction and Analysis on Source Resistance in $In_{0.8}Ga_{0.2}As$ QW HEMTs Considering Ballistic Transport** Se-Hun Kim, Mun-Ho Kim, Min-Kyu Song, Seung-Woo Son, Su-Min Choi, Min-Seo Yu, In-Geun Lee, Jae-Hak Lee, and Dae-Hyun Kim School of Electronic and Electrical Engineering, Kyungpook National University

TN2-G-7 12:25-12:40	**Saturation Current Ratio Method for Extraction of Parasitic Resistances with Dual Configurations in Individual MISFETs** Ji Won Park[1], Seonghyeon Jeong[1], Seung Hyeop Han[1], Hanbin Lee[1], Gyeongsu Min[1], Hyo-In Yang[1], So-Jeong Park[1], Jun-Ho Jang[1], Jeong Yeon Im[1], Dae Hwan Kim[1], Jong-Ho Bae[1], Dong Myong Kim[2], and Sung-Jin Choi[1] [1]School of Electrical Engineering, Kookmin University, [2]Department of Advanced Technology, DGIST