제 32회 한국반도체학술대회
The 32nd Korean Conference on Semiconductors

2025년 **2월 12일(수)-14일(금)** | 강원도 하이원리조트

Future Normal in Semiconductor

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2025년 2월 13일(목), 09:00-10:45

Room J(스페이드 II+III), 6층

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G. Device & Process Modeling, Simulation and Reliability 분과

O10_[TJ1-G] TCAD Simulation

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좌장: 장지원 교수(연세대학교), 백록현 교수(포항공과대학교)

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초청 TJ1-G-1 09:00-09:30	**Impact of Random Discrete Dopants on 6F^2 DRAM Cell Transistors: A Simulation Study** Jaehyun Lee School of Electrical and Electronics Engineering, Pusan National University
TJ1-G-2 09:30-09:45	**Effect of Metal-Capping Layer on Electrical Performances in a-IGZO TFTs: Experiment and TCAD Simulation** Seongbin Lim[1], Soohyun Lim[1], Jaewook Yoo[1], Hyeonjun Song[1], Soyeon Kim[1], Hongseung Lee[1], Minah Park[1], Seohyeon Park[1], Sojin Jung[1], Jin-Ha Hwang[2], Kiyoung Lee[2], Sangmoon Yoon[3], and Hagyoul Bae[1] [1]Jeonbuk National University, [2]Hongik University, [3]Gachon University
TJ1-G-3 09:45-10:00	**Random Phase Distribution Effects of Ferroelectric Tunneling Field-Effect-Transistors (FeTFETs)** Jiwon Park and Woo Young Choi Department Electrical and Computer Engineering and ISRC, Seoul National University
TJ1-G-4 10:00-10:15	**Assessment of Logic Circuit Characteristics with Contact Resistance in 2D Material-Based Complementary-FETs (CFETs)** Hanggyo Jung[1] and Jongwook Jeon[2] [1]Department of Semiconductor Convergence Engineering, Sungkyunkwan University, [2]School of Electronic and Electrical Engineering, Sungkyunkwan University
TJ1-G-5 10:15-10:30	**Comprehensive Analysis of Random Variability in Forksheet FETs Compared to Nanosheet FETs** Minchan Kim, Seunghwan Lee, Junjong Lee, Sanguk Lee, Yonghwan Ahn, Gunryeol Cho, and Rock-Hyun Baek Department of Electrical Engineering, POSTECH

J1-G-6 10:30-10:45	**A Novel Simulation Method of Harmonic Distortion of RF Substrates using Ramo-Shockley Theorem** Nakwon Yu, Jongmin Kim, Youngchul Kim, and Hyunchul Nah TE Team, DB HiTek