



## Future Normal in Semiconductor

2025년 2월 13일(목), 09:00-10:45

Room B(그랜드볼룸III), 4층

### K. Memory (Design & Process Technology) 분과

### 002\_[TB1-K] Charge Trapped Memory Application - I

좌장: 강대웅 교수(서울대학교), 전종욱 교수(성균관대학교)

<p><b>초청</b> TB1-K-1 09:00-09:30</p>	<p><b>Key Challenges of VNAND Unit Cell Design for Higher Layer Stacking</b> Doo Hee Hwang, Sang Hoon Kim, Seung Jae Baik, and Jae duk Lee Flash TD Team, Semiconductor R&amp;D Center, Samsung Electronics Co., Ltd.</p>
<p>TB1-K-2 09:30-09:45</p>	<p><b>Array-level NAND Cell Simulator for Feasibility Assessment of Novel Memory Cells in 3D NAND Architecture</b> Seong Hwan Kong and Wonbo Shim Seoul National University of Science and Technology</p>
<p>TB1-K-3 09:45-10:00</p>	<p><b>Improved Memory Characteristics of MONOS Device with High-k dots Embedded Si<sub>3</sub>N<sub>4</sub> Charge Trap Layer</b> Seongho Lee<sup>1</sup>, San Park<sup>1</sup>, Sehyeon Choi<sup>1</sup>, Yun Seo Lim<sup>1</sup>, Hyungjun Kim<sup>2</sup>, Jaehyun Yang<sup>2</sup>, Bio Kim<sup>2</sup>, Youngseon Son<sup>2</sup>, Hanmei Choi<sup>2</sup>, and Changhwan Choi<sup>1</sup> <sup>1</sup>Division of Materials Science &amp; Engineering, Hanyang University, <sup>2</sup>Memory Process Development Team, Samsung Electronics Co., Ltd.</p>
<p>TB1-K-4 10:00-10:15</p>	<p><b>Analysis of the Dominant Mechanism in Hybrid NAND Flash for Enhanced Memory Window</b> Jaeseon Eo<sup>1</sup>, Kihoon Nam<sup>1</sup>, Donghyun Kim<sup>1</sup>, Jiyeon Kim<sup>1</sup>, Sanghun Jeon<sup>2</sup>, and Rock-Hyun Baek<sup>1</sup> <sup>1</sup>Department of Electrical Engineering, POSTECH, <sup>2</sup>School of Electrical Engineering, KAIST</p>
<p>TB1-K-5 10:15-10:30</p>	<p><b>Leveraging Negative Capacitance for Reducing Operating Voltage in High-Density 3D NAND Technology</b> Sangho Lee, Yunseok Nam, Giuk Kim, Hunbeom Shin, Seokjoong Shin, and Sanghun Jeon School of Electrical Engineering, KAIST</p>



# 제 32회 한국반도체학술대회

The 32nd Korean Conference on Semiconductors

2025년 2월 12일(수)-14일(금) | 강원도 하이원리조트

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TB1-K-6 10:30-10:45	Unveiling the Origin of Disturbance in FeFET and the Potential of Multifunctional TiO <sub>2</sub> as a Breakthrough for Disturb-free 3D NAND Cell Hyunjun Kang, Giuk Kim, and Sanghun Jeon School of Electrical Engineering, KAIST
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