2025년 2월 13일(목), 15:50-17:20
Room A(그랜드볼룸 I), 4층

K. Memory (Design & Process Technology) 분과

O27_[TA3-K] Charge Trapped Memory Technology - II

좌장: 백승재 마스터(삼성전자), 강명곤 교수(서울시립대학교)

초청 TA3-K-1 15:50-16:20	**Development Trend for Cell Structure Having More 500 Layers in 3D NAND Flash** Daewoong Kang Seoul National University
TA3-K-2 16:20-16:35	**Predictive Modeling of Erase Characteristics in 3D V-NAND Memory through Physical Analysis and Machine Learning** In-Je Song[1,2], Tae-Hyun Park[3], Ga-Min Gwon[3], and Ji-Woon Yang[2,3] [1]Global QRA, SK Hynix Inc., [2]Department of Semiconductor Convergence Engineering, Korea University, [3]Department of Electronics & Information Engineering, Korea University
TA3-K-3 16:35-16:50	**Effect of Source Underlap on Hot Electron Injection of Charge-Trapping Tunnel Field Effect Transistors** Seon Ho Lee, Hyung Jun Noh, Chang Heon Park, Minseok Cha, and Woo Young Choi Department of Electrical and Computer Engineering, Seoul National University
TA3-K-4 16:50-17:05	**Analysis of Program Operation Characteristics Induced by Process Variation of Channel Hole Etch in 3D Nand Flash Memory** Won-seop Choi[1,3], In-Je Song[2,3], Tae-Hyun Park[4], Chae-Young Kim[4], Seung-Hyeon Kim[4], Ga-Min Gwon[4], and Ji-Woon Yang[3,4] [1]Nand Plug Etch Technology, SK Hynix Inc., [2]Global QRA, SK Hynix Inc., [3]Department of Semiconductor Convergence Engineering, Korea University, [4]Department of Electronics & Information Engineering, Korea University
TA3-K-5 17:05-17:20	**Memory Characteristics of Flash Memory Using TiN Metal-Dot Embedded SiN_x Charge Trap Layer** Yun Seo Lim[1], San Park[1], Se Hyeon Choi[1], Bon Cheol Ku[1], Seong Ho Lee[1], Hyung Jun Kim[2], Jae Hyun Yang[2], Bio Kim[2], Young Seon Son[2], Han Mei Choi[2], and Chang Hwan Choi[1] [1]Division of Materials Science & Engineering, Hanyang University, [2]Memory Process Development Team, Samsung Electronics Co., Ltd.