2025년 2월 14일(금), 10:55-12:40
Room K(하트 I), 6층

K. Memory (Design & Process Technology) 분과

O63_[FK2-K] Ferroelectric and Oxide Channel based Memory Technology

좌장: 김성준 교수(동국대학교), 양승열 마스터(SAIT)

FK2-K-1 10:55-11:10	Application-Dependent Bias Scheme Optimization for Ferroelectric-Tunnel-FET-Based One-Transistor Ternary Content-Addressable Memory Minjeong Ryu[1,2], Jae Seung Woo[1,2], Yeonwoo Kim[1,2], and Woo Young Choi[1,2] [1]Department Electrical and Computer Engineering, Seoul National University, [2]Inter-university Semiconductor Research Center, Seoul National University
FK2-K-2 11:10-11:25	Achieving Low-Voltage Operation of 1T-nC FRAM Via Precise Engineering of Polarization Switching Kinetics in Hafnia Ferroelectrics Sangho Lee, Giuk Kim, Chaeheon Kim, Yunseok Nam, Junghyeon Hwang, Hunbeom Shin, Seokjoong Shin, and Sanghun Jeon School of Electrical Engineering, KAIST
FK2-K-3 11:25-11:40	The Opportunity of Anti -ferroelectrics in FeFET for the Emerging Non-volatile Memory Applications School of Electrical Engineering, KAIST
FK2-K-4 11:40-11:55	Comparison of Bi-Layer and Tri-Layer Structures in ZrO_2/ZnO/HfO_2 Synaptic Devices for Improved Neuromorphic Performance Dong-Min Kim[1], Yu-Bin Kim[1], Sung-Ho Kim[1], Chae-Min Yeom[1], Shivam Kumar Gautam[1], Hyuk-Min Kwon[2], Yong-Goo Kim[3], and Hi-Deok Lee[1] [1]Department of Electronics Engineering, Chungnam National University, [2]School of Electronic & Electrical Engineering, Hankyong National university, [3]Department of Green Semiconductor System, Korea Polytechnics
FK2-K-5 11:55-12:10	Study of IGZO-Based CTF Memory With State Updates In Array Ria Choi[1], Eunpyo Park[2], Heerak Wi[1], Dae Kyu Lee[2], Min Jee Kim[2], and Joon Young Kwak[1] [1]Ewha Womans University, [2]KIST

FK2-K-6 12:10-12:25	Electrically Erasable Oxide-Semiconductor-Channel Charge Trap Flash Memory with Unipolar Operation Chanyeong Go[1], Seongmin Park[1], and Yoonyoung Chung[1,2,3] [1]Department of Electrical Engineering, POSTECH, [2]Department of Semiconductor Engineering, POSTECH, [3]Center for Semiconductor Technology, POSTECH