2025년 2월 14일(금), 09:00-10:45
Room H(루비 I), 5층

F. Silicon and Group-IV Devices and Integration Technology 분과

## O48_[FH1-F] 3D GAA/CFET Technology

좌장: 정규원 교수(서울대학교), 김시현 교수(서강대학교)

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| FH1-F-1<br>09:00-09:15 | **Low-Temperature Fabrication of Silicon Nanowire GAAFETs with Excimer Laser Recrystallization for M3D Integration**<br>Jeong Yeon Im[1], Hanbin Lee[1], Gyeongsu Min[1], Hyo-In Yang[1], So Jeong Park[1], Jun-Ho Jang[1], Ji Won Park[1], Seonghyeon Jeong[1], Dae Hwan Kim[1], Jong-Ho Bae[1], Dong Myong Kim[3], Min-Ho Kang[2], and Sung-Jin Choi[1]<br>[1]School of Electrical Engineering, Kookmin University, [2]Department of Nano-process, National Nanofab Center, [3]Department of Advanced Technology, DGIST |
| FH1-F-2<br>09:15-09:30 | **Strained Ge/Si Heterogeneous 3D Sequential CFET Featuring First Strain Engineered Ge Top Channel**<br>Hyeongrak Lim[1], Seong Kwang Kim[1], Seung Woo Lee[1], Youngkeun Park[1], Jaejoong Jeong[1], Hojin Jeong[1], Jinha Lim[1], Dae-Myeong Geum[2], Jaehoon Han[3], Younghyun Kim[4], Jaeyong Jeong[1], Byung Jin Cho[1], and Sanghyeon Kim[1]<br>[1]KAIST, [2]Inha University, [3]KIST, [4]Hanyang University |
| FH1-F-3<br>09:30-09:45 | **Photoresponsive GIDL Characterization for Simultaneous Extraction of Donor- and Acceptor-like Interface Trap States in Vertically Stacked Si-NW GAA FETs**<br>Seohyeon Park[1], Donghyeon Lee[1], Jaewook Yoo[1], Minah Park[1], Hongseung Lee[1], Hyeonjun Song[1], Soyeon Kim[1], Seongbin Lim[1], Sojin Jung[1], TaeWan Kim[3], Yang Kyu Choi[2], and Hagyoul Bae[1]<br>[1]Jeonbuk National University, [2]KAIST, [3]University of Seoul |
| FH1-F-4<br>09:45-10:00 | **Transient Analysis of CFET Inverter with Backside Interconnections : Buried Power Rails, Bottom Contacts**<br>Seung-Woo Jung and Sung-Min Hong<br>School of Electrical Engineering and Computer Science, GIST |

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| FH1-F-5<br>10:00-10:15 | **Implementation of a Stress Calculation Module in an In-House Process Emulator for Monolithic CFET**<br>Min-Seo Jang[1], In Ki Kim[1], Seung-Woo Jung[1], Jeong Hyeon Yun[2], Myoung Jin Lee[2], and Sung-Min Hong[1]<br>[1]School of Electrical Engineering and Computer Science, GIST, [2]Department of Electronic Engineering, Chonnam National University |
| FH1-F-6<br>10:15-10:30 | **A Novel 3D-SRAM Architecture based on VGAA Transistors for Advanced AI and Edge Computing Applications**<br>Changwoo Han and Changhwan Shin<br>School of Electrical Engineering, College of Engineering, Korea University |
| FH1-F-7<br>10:30-10:45 | **Multi-$V_{th}$ Through Different Inner Gates Work Functions**<br>Seungjoon Jeong, Haevin Choi, and Changhwan Shin<br>School of Electrical Engineering, Korea University |