2025년 2월 14일(금), 15:10-17:10
Room D(에메랄드 I), 5층

A. Interconnect & Package 분과

O70_[FD3-A] Advanced Package 2

좌장: 주지호 책임(한국전자통신연구원), 이소연 교수(대한민국연구원)

FD3-A-1 15:10-15:25	대기압 기화 플라스마를 이용한 웨이퍼 본딩 기술 Wonyoung Choi, Bumki Moon, Jungshin Lee, Yongjoo Lee, Byeongtak Park, Seung ho Han, Nungpyo Hong, and Kyeongbin Lim Semiconductor R&D Center, Samsung Electronics Co., Ltd.
FD3-A-2 15:25-15:40	TEOS SIO_2 Film Deposition Optimization for Increasing Capability and Securing TSV Robustness of HBM Intae Whoang[1], Byung Yoon Lim[2], Kijun Bang[2], and Sang Un Lee[2] SK hynix
FD3-A-3 15:40-15:55	Crystal Plasticity-Based Modeling of the Influence of Microstructures and Grain Boundary Junction Types on the Cu-Cu Bonding Interface. Jae-Uk Lee[1], Hyun-Dong Lee[1], Sung-Hyun Oh[1], Jihun Kim[1], Ki-Beom Kim[2], Ho-Jin Lee[3], Yeon-Su Kim[2], Gyeong-Bim Lim[3], Sarah-Eunkyung Kim[4], Hoo-Jeong Lee[1], and Eun-Ho Lee[1] [1]Sungkyunkwan University, [2]Sk Hynix, [3]Samsung Electronics,[4]Seoul National University of Science of Technology
FD3-A-4 15:55-16:10	Drive Circuit for Semiconductor Die Testing and Applications Youngwoo Yoo and Young-Joon Kim Gachon University
FD3-A-5 16:10-16:25	An Efficient Standardized Simulation Model for Evaluation of Board Level Reliability in Semiconductor Applications Jaehee An[1], Wan-Kyu Choi[2], and Sangyul Ha[1] [1]Department of Semiconductor Engineering, MyongJi University, [2]DRAM Module Solution, SK hynix

FD3-A-6 16:25-16:40	**Advanced Cu/Polymer Hybrid bonding for 3D Multi-chip Stacking Process** Jihun Kim and Jong Kyoung Park Department of Semiconductor Engineering, Seoul National University of Science and Technology
FD3-A-7 16:40-16:55	**Digital Design and DOE-Based Analysis for Optimal Wire Configuration in Diode Modules** Na-Yeon Choi[1,2] and Sung-Uk Zhang[1,2] [1]Digital Twin Laboratory, Dong-Eui University, [2]Center for Brain Busan 21 Plus Program