2025년 2월 14일(금), 09:00-10:45
Room D(에메랄드 I), 5층

Q. Metrology, Inspection, Analysis, and Yield Enhancement 분과

O44_[FD1-Q] Metrology, Inspection, Analysis, and Yield Enhancement I

좌장: 강상우 소장(한국표준과학연구원), 정용우 TL(SK 하이닉스)

초청 FD1-Q-1 09:00-09:30	Thickness Measurement of Metal Layers via Photoacoustic Waves Induced by Femtosecond Pulses Woojeong Lee, Seung-Yu Jeong, Yeo-Jun Park, and Joohyung Lee Department of Mechanical System Design Engineering, Seoul National University of Science and Technology
초청 FD1-Q-2 09:30-10:00	반도체 FEB에서의 공정 기준에 대한 고찰 부제 : In Line SEM의 Application별 필요 기준이 무엇이며 어떤 문제점이 있는지 알아보자. 양경모 하이케이엠 주식회사
초청 FD1-Q-3 10:00-10:30	Predicting Embedded Silicon-Germane(eSiGe) Defects in Foundry PMOSFET Devices Using Machine Learning Techniques Caused by Outdoor Nanoparticles Jongmin Lee[1,2], Jungtae Park[1,2], Il-Jin Kim[2], Haeun Lee[2], and Sehoon Park[2] [1]Department of Materials Science and Engineering, Yonsei University, [2]Samsung Electronics Co., Ltd.
FD1-Q-4 10:30-10:45	A High Density Full Wafer Structure Measurement Method based on Imaging Ellipsometry for Process Uniformity Control Jinwoo Ahn[1], Hyukjoon Cho[1], Jaehyun Son[1], Changhyeong Yoon[1], Ji Yong Shin[1], Juntaek Oh[1], Donggun Lee[1], Seunga Lim[1], Eunsoo Hwang[1], Jinsoo Lee[1], Jaewon Lee[1], Taeyong Jo[1], Jihye Lee[2], Younghoon Sohn[3], and Myungjun Lee[1] [1]Advanced Process Development Team [4], Semiconductor R&D Center, Samsung Electronics Co., Ltd, [2]DRAM Process Architecture Team, DRAM Product & Technology Technology, Samsung Electronics Co., Ltd, [3]Metrology & Inspection Technology Team, Common Tech Center, Samsung Electronics Co., Ltd,