2025년 2월 14일(금), 09:00-10:45
Room B(그랜드볼룸III), 4층

K. Memory (Design & Process Technology) 분과

O42_[FB1-K] Ferroelectric Memory Technology

좌장: 김윤 교수(서울시립대학교), 심원보 교수(서울과학기술대학교)

FB1-K-1 09:00-09:15	**Vertical Self-Rectifying Ferroelectric Tunnel Junction-based 3D Content Addressable Memory for Data-Centric Computing** Chaeheon Kim, Junghyeon Hwang, Yongsu Kim, and Sanghun Jeon School of Electrical Engineering, KAIST
FB1-K-2 09:15-09:30	**Enhanced Non-Volatile Memory Performance in CNT-FeFETs with Zr-Doped HfO_2 Ferroelectric Layer** So-Jeong Park[1], Hanbin Lee[1], Hyo-In Yang[1], Gyeongsu Min[1], Jun-Ho Jang[1], Jeong Yeon Im[1], Ji Won Park[1], Seonghyeon Jeong[1],Dae Hwan Kim[1], Jong-Ho Bae[1], Min-Ho Kang[2], Dong Myong Kim[3], and Sung-Jin Choi[1] [1]School of Electrical Engineering, Kookmin University, [2]Department of Nano-process, NNFC, [3]Department of Advanced Technology, DGIST
FB1-K-3 09:30-09:45	**Analysis of Leakage-Current-Assisted Polarization Mechanism for Memory Window Expansion in Ferroelectric a-InGaZnO_x Thin Film Transistor** Sujong Kim[1], Ha-Neul Lee[1], Hyojin Yang[1], Hwan Jin Kim[1], Hyunwook Jeong[1], Yubin Choi[1], Sung-Jin Choi[1], Dong Myong Kim[2], Dae Hwan Kim[1], Sung Yun Woo[3], and Jong-Ho Bae[1] [1]School of Electrical Engineering, Kookmin University, [2]Department of Advanced Technology, DGIST, [3]School of Electronic and Electrical Engineering, Kyungpook National University
FB1-K-4 09:45-10:00	**Investigation of Memory Operations in InGaAs MFMIS Tunnel FET** Kyul Ko[1,2], Dae-Hwan Ahn[1], Jai-Youn Jeong[1], Byeong-Kwon Ju[2], and Jae-Hoon Han[1] [1]KIST, [2]Korea University

FB1-K-5 10:00-10:15	Low EOT & Leakage HZO Capacitor (EOT:3.6Å&J_{leak}:7×10^{-8}A/cm^2@0.8V) Enabled by Low-Temperature & Dielectric-Selective Microwave Annealing Hunbeom Shin, Giuk Kim, Sujeong Lee, Geonhyeong Kang, Hyojun Choi, Taeseung Jung, Sangho Lee, and Sanghun Jeon School of Electrical Engineering, KAIST
FB1-K-6 10:15-10:30	Low-Voltage and QLC NAND Flash Device Enabled by Hafnia Ferroelectric Layer: Experimental Validation and Modeling Giuk Kim, Hyojun Choi, and Sanghun Jeon School of Electrical Engineering, KAIST
FB1-K-7 10:30-10:45	Impact of the Starting Layer on the Electrical Properties of Superlattice HZO Jaemin Yeom[1], Jun bum Lee[1,2], and Woo Young Choi[1] [1]Department of Electrical and Computer Engineering, Seoul National University, [2]DRAM Technology Development, Semiconductor R&D Center, Samsung Electronics Co., Ltd.