2024년 1월 25일(목), 10:55-12:40
Room H(202),2층

K. Memory (Design & Process Technology) 분과
[TH2-K] DRAM

좌장: 오정훈 마스터(삼성전자)

초청발표 TH2-K-1 10:55-11:25	Improvement of DRAM Cell Data Sensing Margin by Retargeting Local Misalignment and Process Skew Kyuseok Lee[1], Jungyoung Koh[1], Hyunju Sung[1], Jaehyun Yu[1], Hyunmi Ji[1], Yeongeun Kim[1], Hyewon Kim[1], Jae Bum Jeon[1], Jiseong Jeong[1], Sunha Baek[2], Ohhun Kwon[2], and Jemin Park[1] [1]Semiconductor R&D Center, Samsung Electronics Co., Ltd., [2]Design Technology Team, Samsung Electronics Co., Ltd.
초청발표 TH2-K-2 11:25-11:55	Challenges and Issues of 2T-0C Device for DRAM Applications with Respect to Write/Read Operation and 3D Cell Architectures Dae Hwan Kang[1,4], Juyoung Yun[2], Suwon Seong[2], Beongwoo Lee[3], Junyoung Choi[3], Jimin Lee[3], Min-Su Cho[2], Yoonyoung Chung[1,2,4], Sung Woong Chung[1,4], and Seyoung Kim[1,3,4] [1]Department of Semiconductor Engineering, POSTECH, [2]Department of Electrical Engineering, POSTECH, [3]Department of Materials Science and Engineering, POSTECH, [4]CSTC, POSTECH
TH2-K-3 11:55-12:10	Computational Device Design of Cylindrical IGZO 2T0C DRAM Cell Sang-Mok Jeong and Sung-Min Hong School of Electrical Engineering and Computer Science, GIST
TH2-K-4 12:10-12:25	Mitigating Leakage Current Issues in 1-Row Hammer by Introducing Buried Oxide under the BCAT Structure Sang Hyun Lee, Yeon Seok Kim, Chang Young Lim, and Min-Woo Kwon Department of Electric Engineering, Gangneung-Wonju National University
TH2-K-5 12:25-12:40	A Novel 2T0C DRAM Cell Structure and Refresh Technique for Processing-in-memory Applications Seong Hwan Kong, Hui-Jae Choi, Chan-Gi Yook, and Wonbo Shim Seoul National University of Science and Technology