



제 31회 한국반도체학술대회

The 31st Korean Conference on Semiconductors

2024년 1월 24일(수)-26일(금) | 경주화백컨벤션센터(HICO)

2024년 1월 25일(목), 09:00-10:45

Room C(103), 1층

J. Nano-Science & Technology 분과

[TC1-J] van der Waals Heterostructure Electronics

좌장: 이관형 교수(서울대학교), 이명재 교수(서울대학교)

<p>초청발표</p> <p>TC1-J-1</p> <p>09:00-09:30</p>	<p>2D Materials Design for Angstrom-scale Multi-stack Devices</p> <p>Hyeon-Jin Shin</p> <p>SAIT</p>
<p>TC1-J-2</p> <p>09:30-09:45</p>	<p>NMOS Inverter based on Vertically Stacked MoS₂ n-MOSFET Using Semi-metallic PtSe₂ Contacts</p> <p>Jae Eun Seo¹, Minseung Gyeon², Jisoo Seok¹, Kibum Kang², and Jiwon Chang¹</p> <p>¹Department of System Semiconductor Engineering and Department of Materials Science and Engineering, Yonsei University, ²Department of Materials Science and Engineering, KAIST</p>
<p>TC1-J-3</p> <p>09:45-10:00</p>	<p>Atomic-Thin Dielectric Integration with Hexagonal Boron Nitride for Large Scale MoS₂ Field Effect Transistors</p> <p>Woo-Ju Lee^{1,2}, Min-Yeong Choi^{1,2}, Seong-Jun Yang¹, and Cheol-Joo Kim^{1,2}</p> <p>¹Center for Van der Waals Quantum Solids, IBS, ²Department of Chemical Engineering, POSTECH</p>
<p>초청발표</p> <p>TC1-J-4</p> <p>10:00-10:30</p>	<p>Reliable Transistors Fabricated via Two-dimensional Layer Transfer Assisted Heterogeneous Integration Techniques</p> <p>Hyun S. Kum</p> <p>Yonsei University</p>
<p>TC1-J-5</p> <p>10:30-10:45</p>	<p>Two-dimensional Layer Induced Resistive Switching Properties of Hafnia-Based Heterostructure</p> <p>Donghyeon Lee¹, Seungmo Kim^{2,3}, and Sanghan Lee¹</p> <p>¹School of Materials Science and Engineering, GIST, ²Center for Semiconductor Technology Convergence, POSTECH, ³Department of Electrical Engineering, POSTECH</p>