2024년 1월 26일(금), 13:45-15:30
Room K(205),2층

G. Device & Process Modeling, Simulation and Reliability 분과

[FK2-G] TCAD & Compact Modeling

좌장: 최성진 교수(국민대학교), 김현우 교수(건국대학교)

초청발표 FK2-G-1 13:45-14:15	Enhancing AC Degradation Modeling by considering the Degradation Profile Induced by DC Stress in SiON pMOSFETs Yeohyeok Yu Department of Information and Communication Technology Engineering, Jeonju University
FK2-G-2 14:15-14:30	Physical Compact Model of Double-Gate MOSFET with a-IGZO Channel for Cell Array Transistor in 3-Dimensional DRAM Tae-Hyun Park and Ji-Woon Yang Department of Electronics and Information Engineering, Korea University
FK2-G-3 14:30-14:45	Quasi 2-Dimensional Compact Model of Channel-All-Around MOSFETs for 3-Dimensional DRAM Chae-Young Kim and Ji-Woon Yang Department of Electronics and Information Engineering, Korea University
FK2-G-4 14:45-15:00	Intrinsic Delay Optimization on Lateral Source/Drain Growth Profile for NanosheetField-effect Transistor Jae Woog Jung, Hwi Seung Park, and Hyun Woo Kim Department of Electrical and Electronics Engineering, Konkuk University
FK2-G-5 15:00-15:15	Exploring the Impact of Channel Tapered Angle and Number of Channel Stacks in Nanosheet and Forksheet FETs Yonghwan Ahn, Junjong Lee, Jinsu Jeong, Seunghwan Lee, Sanguk Lee, and Rock-Hyun Baek Department of Electrical Engineering, POSTECH
FK2-G-6 15:15-15:30	Accelerated Device Simulation of Gate-all-around Nanosheet MOSFETs Using Quasi-1D Model Kwang-Woon Lee and Sung-Min Hong School of Electrical Engineering and Computer Science, GIST