



# 제 31회 한국반도체학술대회

The 31st Korean Conference on Semiconductors

2024년 1월 24일(수)-26일(금) | 경주화백컨벤션센터(HICO)

2024년 1월 26일(금), 13:45-15:30

Room G(201), 2층

## K. Memory (Design & Process Technology) 분과

### [FG2-K] Charge Trap Flash Memory

좌장: 우성윤 교수(경북대학교), 정연주 박사(KIST)

<p>FG2-K-1 13:45-14:00</p>	<p>A Fully Logic-compatible High-k Charge Trap Memory for sub-28nm Embedded Non-volatile Memory Technologies Jaehun Lee, Kyongsik Yeom, Jongsung Woo, Hyunik Park, Han-Hyeong Choi, Donghwi Hwang, Minji Seo, Hwanho Ma, Jeadong Jung, Jusang Lee, Juwoon Kim, Youngcheon Jeong, Changmin Jeon, Kangho Lee, and Hyunjo Kim Samsung Foundry, Samsung Electronics Co., Ltd.</p>
<p>FG2-K-2 14:00-14:15</p>	<p>Low-power Split-gate NOR Flash Cell Design and Non-ideality Analysis for Compute-in-memory Chan-Gi Yook, Seung-won Lee, and Wonbo Shim Seoul National University of Science and Technology</p>
<p>FG2-K-3 14:15-14:30</p>	<p>고분자 iCVD 증착 기술을 이용한 불소 도핑에 의한 a-InGaZnO 박막 트랜지스터 소자 특성 향상 오승현<sup>1</sup>, 이창현<sup>2</sup>, 조성행<sup>3</sup>, 김희태<sup>1</sup>, 박정익<sup>2</sup>, 김민주<sup>4</sup>, 박영근<sup>1</sup>, 정민규<sup>5</sup>, 박세준<sup>5</sup>, 임성갑<sup>2</sup>, 조병진<sup>1</sup> <sup>1</sup>한국과학기술원 전기 및 전자공학부, <sup>2</sup>한국과학기술원 신소재공학부, <sup>3</sup>한국전자통신연구원 플렉시블전자소자연구실, <sup>4</sup>단국대학교 전자전기공학부, <sup>5</sup>Samsung Electronics Co., Ltd.</p>
<p>FG2-K-4 14:30-14:45</p>	<p>Augmenting the Memory Window of Charge Trap Flash through Sputtering Substrate Bias-Induced Trap Generation Hyunyoung Cho<sup>1</sup>, Seongmin Park<sup>1</sup>, and Yoonyoung Chung<sup>1,2,3</sup> <sup>1</sup>Department of Electrical Engineering, POSTECH, <sup>2</sup>Department of Semiconductor Engineering, POSTECH, <sup>3</sup>Center for Semiconductor Technology Convergence, POSTECH</p>
<p>FG2-K-5 14:45-15:00</p>	<p>Improvement on Program/Erase Performance of Amorphous Indium-gallium-zinc-oxide-Based Charge Trap Memory via TCAD Simulation Gyeongsu Min<sup>1</sup>, Hanbin Lee<sup>1</sup>, Yulim An<sup>1</sup>, Jeonghee Ko<sup>1</sup>, Hyo-In Yang<sup>1</sup>, So Jeong Park<sup>1</sup>, Jun-Ho Jang<sup>1</sup>, Jeong Yeon Im<sup>1</sup>, Dong Myong Kim<sup>1</sup>, Dae Hwan Kim<sup>1</sup>, Jong-Ho Bae<sup>1</sup>, Min-Ho Kang<sup>2</sup>, and Sung-Jin Choi<sup>1</sup> <sup>1</sup>School of Electrical Engineering, Kookmin University, <sup>2</sup>Department of Nano-process, NNFC</p>



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FG2-K-7

15:00-15:15

Investigation of Bias Temperature Instabilities of Peripheral pMOSFET and nMOSFET in CTF-NAND Flash Memories with COP Structure for Cryogenic Memory Applications

Jung Rae Cho<sup>1</sup>, Jingyu Park<sup>1</sup>, Tae Jun Yang<sup>1</sup>, Seonhaeng Lee<sup>2</sup>, and Dae Hwan Kim<sup>1</sup>

<sup>1</sup>School of Electrical Engineering, Kookmin University, <sup>2</sup>Memory Division, Samsung Electronics Co., Ltd.