2024년 1월 26일(금), 13:45-15:30
Room D(104), 1층

## F. Silicon and Group-IV Devices and Integration Technology 분과 [FD2-F] Advanced Device Characterizations

좌장: 김명수 교수(울산과학기술원), 권지민 교수(울산과학기술원)

| $\begin{aligned} & \text { FD2-F-1 } \\ & \text { 13:45-14:00 } \end{aligned}$ | Multivalued Negative Differential Resistance (NDR) ZnO Channel Thin Film Transistor (TFT) Integrated with $\mathrm{Ag} / \mathrm{HfO}_{2}$ Threshold Switching Device Juho Sung ${ }^{1}$ and Changhwan Shin ${ }^{2}$ <br> ${ }^{1}$ Department of Electrical and Computer Engineering, Sungkyunkwan University, ${ }^{2}$ School of Electrical Engineering, Korea University |
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| $\begin{aligned} & \text { FD2-F-2 } \\ & \text { 14:00-14:15 } \end{aligned}$ | Investigation of Interface Trap Effect in Feedback Field Effect Transistor <br> Hangwook Jeong, Minseon Park, Junhyeong Lee, and Min-Woo Kwon Department of Electronic Engineering, Gangneung-Wonju National University |
| $\begin{aligned} & \text { FD2-F-3 } \\ & \text { 14:15-14:30 } \end{aligned}$ | Steep Slope Transistor with Negligible Hysteresis Achieved through <br> Transient Negative Capacitance <br> Sangho Lee, Giuk Kim, Hunbeom Shin, Yunseok Nam, and Sanghun Jeon <br> School of Electrical Engineering, KAIST |
| $\begin{aligned} & \text { FD2-F-4 } \\ & \text { 14:30-14:45 } \end{aligned}$ | Design and Characterization of a Double-Trench SiC MOSFET with Superb Current Rectification <br> Yu Jin Kang and Seongjae Cho <br> Department of Electronic and Electrical Engineering, Ewha Womans University |
| $\begin{aligned} & \text { FD2-F-5 } \\ & \text { 14:45-15:00 } \end{aligned}$ | 3D Analysis Methodology for Line Edge Roughness in V-NAND Structure <br> Jaehyuk Lim ${ }^{1}$ and Changhwan Shin ${ }^{2}$ <br> ${ }^{1}$ Department of Electrical and Computer Engineering, Sungkyunkwan University, ${ }^{2}$ School of Electrical Engineering, Korea University |
| $\begin{aligned} & \text { FD2-F-6 } \\ & \text { 15:00-15:15 } \end{aligned}$ | Enhancement Thermal Performance of Drain-extended FinFETs for SOC Applications <br> Yeon Sil Yang and Jang Hyun Kim <br> Department of Intelligence Semiconductor Engineering, Ajou University |

