2022년 1월 26일(수), 15:45-17:30
Room L (다이아몬드 II, 6층)

N. VLSI CAD 분과
[WL4-N] New Devices and Hardware with CAD

좌장: 송대건 교수(경북대학교), 장경욱 교수(성균관대학교)

WL4-N-1 **15:45-16:00**	**A Novel Ternary Logic Gates Implementation, Using Anti-Ambipolar Transistors(AAT) and PMOSs** Jongbeom Kim[1] and Taigon Song[1,2] *[1]School of Electronics Engineering, Kyungpook National University, [2]School of Electronic and Electrical Engineering, Kyungpook National University*
WL4-N-2 **16:00-16:15**	**Standard Cell Design Methodology for Complementary FETs (CFETs)** Eunbin Park[1] and Taigon Song[1,2] *[1]School of Electronics Engineering, Kyungpook National University, [2]School of Electronic and Electrical Engineering, Kyungpook National University*
WL4-N-3 **16:15-16:30**	**Buried Power Rail Schemes Analysis in 3nm Layout** Taehak Kim and Taigon Song *School of Electronic and Electrical Engineering, Kyungpook National University*
WL4-N-4 **16:30-16:45**	**Low Power Ternary Logic Circuit Using Depletion-type MOSFET** Hyundong Lee[1] and Taigon Song[1,2] *[1]School of Electronics Engineering, Kyungpook National University, [2]School of Electronic and Electrical Engineering, Kyungpook National University*
WL4-N-5 **16:45-17:00**	**T-CMOS 를 이용한 최적의 삼진 순차회로 설계** Jonghyun Ko[1] and Taigon Song[1,2] *[1]School of Electronic and Electrical Engineering, Kyungpook National University, [2]School of Electronics Engineering, Kyungpook National University*
WL4-N-6 **17:00-17:15**	**Power Efficiency Analysis of DC-DC Converters in XMODEL** Piljun Jeong[1] and Jaeha Kim[2] *[1]Inter-University Semiconductor Research Center, Seoul National University, [2]Department of Electrical and Computer Engineering, Seoul National University*
WL4-N-7 **17:15-17:30**	**Data Bus Inversion Encoder Hardware Design for Serializer-Containing Data Bus Scheme** Seongyoon Kang and Jongsun Park *Department of Semiconductor System Engineering, Korea University*