



제 29회 한국반도체학술대회

The 29th Korean Conference on Semiconductors

2022년 1월 24일(월)~ 26일(수) | 강원도 하이원 그랜드호텔(컨벤션타워)

2022년 1월 26일(수), 15:45-17:30

Room K (다이아몬드 I, 6층)

F. Silicon and Group-IV Devices and Integration Technology 분과 [WK4-F] 3D Integration Technology

좌장: 김명수 교수(UNIST)

<p>WK4-F-1 15:45-16:00</p>	<p>The Process Development for Monolithic 3D Integration Using Large-Scale Silicon-On-Insulator (SOI) Wafer Bonding Hyeoncheol Cho¹, Hoonhee Han¹, Jaejoong Jung², Byeongjin Cho², and Changhwan Choi¹ ¹Division of Materials Science and Engineering, Hanyang University, ²Department of Electronic Engineering, KAIST</p>
<p>WK4-F-2 16:00-16:15</p>	<p>저마늄 확산 효과와 결정화 엔지니어링을 통한 3차원 수직 낸드플래시 메모리 용 폴리실리콘 채널 이동도 향상에 관한 연구 Tae In Lee¹, Yun Hee Lee¹, Eui Joong Shin¹, Min Ju Kim¹, Jung Hoon Lee², Jaeduk Lee², and Byung Jin Cho¹ ¹School of Electrical Engineering, KAIST, ²Flash Product & Technology, Samsung Electronics Co., Ltd.</p>
<p>WK4-F-3 16:15-16:30</p>	<p>Green Laser Annealing을 활용한 Monolithic 3D Integration 상부 PMOS 소자 구현과 성능 향상에 대한 연구 Youngkeun Park¹, Semin Noh¹, Jaejoong Jeong¹, Jaecheol Shin², and Byung Jin Cho¹ ¹School of Electrical Engineering, KAIST, ²Laser Process Development, Digital Imaging Technology</p>
<p>WK4-F-4 16:30-16:45</p>	<p>CMOS SPAD의 구조 최적화를 통한 수광 효율 향상 Eunsung Park^{1,2}, Woo-Young Choi¹, and Myung-Jae Lee² ¹Department of Electrical and Electronic Engineering, Yonsei University, ²Post-Silicon Semiconductor Institute, KIST</p>
<p>WK4-F-5 16:45-17:00</p>	<p>Noise Perspective of Low Temperature Gate Oxide Adjustment with Single and Dual Dipole Engineering for 3D Sequential Approach Younggwang Yoon¹, Jacopo Franco², Eddy Simoen², Alessio Spessot², and Naoto Horiguchi² ¹SK Hynix, ²IMEC</p>
<p>WK4-F-6 17:00-17:15</p>	<p>Three-Dimensional Topology Simulation of Vertically Stacked Complementary Field Effect Transistor (CFET) with 5 nm Channel Width In Ki Kim and Sung-Min Hong School of Electrical Engineering and Computer Science, GIST</p>
<p>WK4-F-7 17:15-17:30</p>	<p>Investigation of Effect of Monolithic 3D Inverter Stacked with MOSFETs on Random Dopant Fluctuation Geun Jae Lee^{1,2}, Tae Jun Ahn^{1,2}, and Yun Seop Yu^{1,2} ¹Department of ICT Robot Engineering, Hankyong National University, ²Department of Electrical, Electronic and Control Engineering, Hankyong National University</p>