제 29회 한국반도체학술대회 The 29th Korean Conference on Semiconductors

2022년 1월 24일(월)~ 26일(수) | 강원도 하이원 그랜드호텔(컨벤션타워)

2022년 1월 26일(수), 10:45-12:30 Room K (다이아몬드 I, 6층)

F. Silicon and Group-IV Devices and Integration Technology 분과 [WK2-F] Neuromorphic Device Application

좌장: 권대웅 교수(인하대학교)

| WK2-F-1 10:45-11:00 | Analysis of Bit-Error in Spiking Neural Networks According to Retention Characteristics Taejin Jang, Bosung Jeon, Kyungchul Park, and Byung-Gook Park Department of Electrical Engineering, Seoul National University |
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| WK2-F-2 11:00-11:15 | Spike Duration Adjustable Neuron Circuit for Stable Synaptic Operation Jonghyuk Park ^{1,2} , Kyungchul Park ^{1,2} , Bosung Jeon ^{1,2} , and Byung-Gook Park ^{1,2} ¹ Inter-University Semiconductor Research Center (ISRC), Seoul National University, ² Department of Electrical and Computer Engineering, Seoul National University |
| WK2-F-3 11:15-11:30 | Analog Capacitor-less Neuron Circuit Using Multi-gate Feed Back Field Effect Transistor Jun Hyeong Lee, Misun Cha, Jaehoon Shin, Jooyoung Jeon, and Min-Woo Kwon Department of Electric Engineering, Gangneung-Wonju National University |
| WK2-F-4 11:30-11:45 | Nanoelectromechanical Memory Switches for Binary Neural Networks Hyeontae Bang, Sangjun Lee, Jae Seung Woo, and Woo Young Choi Department of Electronic Engineering, Sogang University |
| WK2-F-5 11:45-12:00 | Floating Gate Based Synaptic Device Using Back Tunneling Mechanism Donghyun Ryu, Junsu Yu, and Byung-Gook Park Inter-University Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University |
| WK2-F-6 12:00-12:15 | Analysis of The Effect of Line Resistance in 3D Synaptic Array on The Accuracy of Spiking Neural Networks Seongbin Oh ^{1,2} , Dooyong Koh ^{1,2} , Soochang Lee ^{1,2} , Byung-Gook Park ^{1,2} , and Jong-Ho Lee ^{1,2} ¹ Department of Electrical and Computer Engineering, Seoul National University, ² ISRC, Seoul National University |
| WK2-F-7 12:15-12:30 | Analog Memristive Devices with an Ion-Implanted Current Limiting Layer for Neuromorphic Computing Keonhee Kim ^{1,2} , Dae Cheol Kang ^{1,2} , Jae Gwang Lim ^{1,2} , Yeonjoo Jeong ¹ , Jaewook Kim ¹ , Suyoun Lee ¹ , Joon Young Kwak ¹ , Jongkil Park ¹ , Gyu Weon Hwang ¹ , Kyeong- Seok Lee ¹ , Byeong-Kwon Ju ² , Jong Keuk Park ¹ , and Inho Kim ¹ ¹ Center for Neuromorphic Engineering, KIST, ² Display and Nanosystem Laboratory, School of Electrical Engineering, Korea University |