2022년 1월 26일(수), 15:45-17:30 Room F (스페이드 I, 6층)

O. System LSI Design 분과 [WF4-O] VLSI Design for Signal Processing

좌장: 김영민 교수(홍익대학교), 김지훈 교수(이화여자대학교)

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WF4-O-1 15:45-16:15	Complexity-Latency Tradeoff for 5G SCL Polar Decoder Architecture 감동윤, 이영주 포항공과대학교 전자전기공학과
WF4-O-2 16:15-16:30	Post-Quantum Cryptography Coprocessor for RISC-V Jihye Lee, Whijin Kim, Sohyeon Kim, and Ji-Hoon Kim Ewha Womans University
WF4-O-3 16:30-16:45	A Low-Cost Voice Recognition System with Embedded Al Accelerator Kwang Hyun Go, Yue Ri Jeong, and Seung Eun Lee Department of Electronic Engineering, Seoul National University of Science and Technology
WF4-O-4 16:45-17:00	Area-Efficient Signal Acquisition for BDS B1C Signals Jiwoon Park, Minsu Kim, and Hoyoung Yoo Chungnam National University
WF4-O-5 17:00-17:15	RISC-V Based Multicore Processor for Smart IoT CCTV Application Seung-Young Lee, Jae-Hyoung Lee, and Woojoo Lee Chung-Ang University
WF4-O-6 17:15-17:30	Multi-mode Transprecision SpMV Engine for PageRank Whijin Kim, Jihye Lee, Sohyeon Kim, and Ji-Hoon Kim Ewha Womans University