2022년 1월 26일(수), 14:00-15:30
Room E (루비 II, 5층)

A. Interconnect & Package 분과
[WE3-A] Advanced Package

좌장: 최광성 책임(ETRI), 김병준 교수(한국산업기술대학교)

WE3-A-1 **14:00-14:30**	**Wafer Level Package Process for HBM** Sung Woo Ma, Minsuk Suh, and Woong-sun Lee *WLP Technology Group, SK Hynix*
WE3-A-2 **14:30-14:45**	**A Study on the Interfacial Reliability of Micro-nano Bimodal Cu Sintered Joints on DBC/AMB Substrates for Power Module** Kirak Son, Aesun Oh, Eunyoung Park, and Hyun-Cheol Bae *DMC Convergence Research Department, ETRI*
WE3-A-3 **14:45-15:00**	**Challenges of Wafer Level Molded Under-Fill for 3D Stacked High Bandwidth Memory** Je Hun Youn, Hyoung Chul Kwon, Seung-Hee Jo, and Woong-Sun Lee *WLP Technology, SK Hynix*
WE3-A-4 **15:00-15:15**	**티타늄 나노 패시베이션을 이용한 저온 구리 웨이퍼 본딩** Seungmin Park[1], Yoonho Kim[1], and Sarrah Eunkyung Kim[2] *[1]Department of Manufacturing System and Design Engineering, Seoul National University of Science and Technology, [2]Department of Semiconductor Engineering, Seoul National University of Science and Technology*
WE3-A-5 **15:15-15:30**	**Effects of Flux Material for MR-MUF Process in Fine Pitch Wafer Level Package** Gi-Tae Moon, Seok-Hyun Hwang, Seung-Hee Jo, and Woong-Sun Lee *WLP Technology, SK Hynix*