2022년 1월 25일(화), 10:45-12:00
Room F (스페이드 I, 6층)

G. Device & Process Modeling, Simulation and Reliability 분과
[TF2-G] Logic Devices and Reliability

좌장: 홍성민 교수(GIST), 백록현 교수(POSTECH)

TF2-G-1 **10:45-11:15**	**Knowledge-Based Neural Compact Model for Semiconductor Device Modeling** Soogine Chong, Chanwoo Park, Ye Sle Cha, Chul-Heung Kim, and Hyunbo Cho *Alsemy Inc.*
TF2-G-2 **11:15-11:30**	**Explicit Surface-Potential Based Compact Model of Negative-Capacitance FETs with MFIS for Accelerated SPICE Simulation** Ju-Hyun Shim and Ji-Woon Yang *Department of Electronics and Information Engineering, Korea University*
TF2-G-3 **11:30-11:45**	**Sensitivity Analysis of each Inner Spacer Thickness Variation in Sub 3-nm Node Silicon Nanosheet Field-Effect Transistors** Sanguk Lee, Jun-Sik Yoon, Jinsu Jeong, Seunghwan Lee, Junjong Lee, Jaewan Lim, and Rock-Hyun Baek *Department of Electrical Engineering, POSTECH*
TF2-G-4 **11:45-12:00**	**FDSOI-Based Polarity Gate-Less Reconfigurable FET** Dong Hyeok Lee[1] and Jiwon Chang[2] *[1]Department of Materials Science & Engineering, Yonsei University, [2]Department of System Semiconductor Engineering, Yonsei University*