2022년 1월 25일(화), 09:00-10:30 Room B (에메랄드 II+III, 5층)

S. Chip Design Contest 분과 [TB1-S] Chip Design Contest

좌장: 이영주 교수(POSTECH), 장영찬 교수(금오공과대학교)

작성: 이성구 표구(POSTECH), 성성선 표구(급포공파대학표)	
TB1-S-1 09:00-09:15	A 60GHz Vector-Sum Phase Shifter Design in TSMC 65nm CMOS Dong Ouk Cho, In Cheol Yoo, and Chul Woo Byeon Department of Electronic Engineering, Wonkwang University
TB1-S-2 09:15-09:30	A Reliable SoC Design using Replica Circuits for Near-Threshold Voltage Operation Hyunchul Park and Jongsun Park Department of Electrical Engineering, Korea University
TB1-S-3 09:30-09:45	A 9 Gb/s/µm Transceiver with a Hybrid ISI and FEXT Equalization Scheme for Next-Generation HBM Interface Kung Ryun Yoon, Seung Woo Park, and Chul Woo Kim Korea University
TB1-S-4 09:45-10:00	A 97.6%-Efficient 1-2MHz Hysteretic Buck Converter with 7V/µs DVS-Rate Enabled by Isosceles-Triangular Shunt Current Push-Pull Technique Hong-Hyun Bae, Jeong-Hyun Cho, Gyeong-Gu Kang, Yousung Park, and Hyun-Sik Kim KAIST
TB1-S-5 10:00-10:15	오동작 감지 회로를 포함하는 능동 EMI 필터 One-chip IC Sangyeong Jeong ^{1,2} and Jingook Kim ^{1,2} ¹ UNIST, ² EMcoretech Co.
TB1-S-6 10:15-10:30	Reset Circuit Design for Multi-pixel THz Imaging System Sang Hyo Ahn, Min Woo Ryu, Minjae Kim, and Kyung Rok Kim Department of Electrical Engineering, UNIST