N. VLSI CAD 분과

2021년 1월 25일(월), 10:45–12:15 / 채널 D

[MD2-N] Design Automation and Optimization

좌장: 강석형 교수 (POSTECH), 송대건 교수 (경북대학교)

MD2-N-1 **10:45-11:15**	[초청] **Circuit Timing Optimization through Selective Use of Airgap IMD** Daijoon Hyun *Cheongju University*
MD2-N-2 **11:15-11:30**	**A GAAFET Library Development at 3nm Node** Tae Hak Kim[1] and Taigon Song[1,2] [1]*School of Electronic and Electrical Engineering, Kyungpook National University,* [2]*School of Electronics Engineering, Kyungpook National University*
MD2-N-3 **11:30-11:45**	**Artificial Netlist Generator for Machine Learning Applications in EDA** Daeyeon Kim, Kyungjun Min, and Seokhyeong Kang *POSTECH*
MD2-N-4 **11:45-12:00**	**Low Power Spiking Neural Network (SNN) Hardware with Prediction Scheme for Embedded Environments** Jeonggyu Yang[1] and Taigon Song[1,2] [1]*School of Electronic and Electrical Engineering, Kyungpook National University,* [2]*School of Electronics Engineering, Kyungpook National University*
MD2-N-5 **12:00-12:15**	**Performance Improvement of Deep-learning HW Using Bit-Level Sparsity** Seunggyu Lee, Eunji Kwon, Yesung Kang, and Seokhyeong Kang *POSTECH*