S. Chip Design Contest 분과

2021년 1월 25일(월), 09:00–10:30 / 채널 D

[MD1-S] Chip Design Contest

좌장: 차혁규 교수 (서울과학기술대학교), 채형일 교수 (건국대학교)

MD1-S-1 **09:00-09:15**	**Low Power ADC Design for Mixed Signal Convolutional Layer Accelerator** JungYeon Lee, DaeHu Park, Malik-Summair Asghar, and HyungWon kim *Department of Electronic Engineering, Chungbuk National University*
MD1-S-2 **09:15-09:30**	**Secure RISC-V SoC for Neural Processing System** Sunyoung Park[1], Hyunji Kim[1], Sung Yeon Kim[2], Wooseok Byun[3], and Ji-Hoon Kim[1] *[1]Department of Electronic and Electrical Engineering, Ewha Womans University, [2]Synopsys Korea, [3]Information and Electronics Research Institute, KAIST*
MD1-S-3 **09:30-09:45**	**A High-Linearity Capacitively Coupled Continuous-Time Delta-Sigma Modulator for Sensor Readout ICs** Chaegang Lim, Yohan Choi, and Chulwoo Kim *Department of Electrical Engineering, Korea University*
MD1-S-4 **09:45-10:00**	**Fully Differential Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 660μA** Ji-Hun Lee and Hyun-Sik Kim *School of Electrical Engineering, KAIST*
MD1-S-5 **10:00-10:15**	**A Class-AB OTA with Slew-Rate Enhancement Technique for High speed Discrete-Time Delta-Sigma Modulator** Seokjae Song and Jeongjin Roh *Division of Electrical Engineering, Hanyang University*
MD1-S-6 **10:15-10:30**	**Time-interleaved Noise-shaping SAR ADC with Redundancy Error Correction Technique** Kihyun Kim[1], Younggyun Oh[2], Seungjun Lee[1], and Hyungil Chae[1] *[1]Department of Electrical Engineering, Konkuk University,* *[2]Department of Electrical Engineering, Kookmin University*