



G. Device & Process Modeling, Simulation and Reliability 분과

2021년 1월 27일(수), 09:00-10:30 / 채널 D

[WD1-G] DTCO and Memory Devices

좌장: 서지웅 팀장 (SK하이닉스), 이재우 교수 (고려대학교)

<p>WD1-G-1 09:00-09:30</p>	<p>[초청] Toward the Material-Device-circuit Co-design of the Oxide Semiconductor-based Artificial Intelligence: from Transistor, Memory, and Sensor to Modeling, Simulation, and Reliability</p> <p>Dae Hwan Kim <i>School of Electrical Engineering, Kookmin University</i></p>
<p>WD1-G-2 09:30-09:45</p>	<p>Design Optimization of FeFET-based TCAM Cell Using Compact Model Combining Ferroelectric Switching and Conventional MOSFETs</p> <p>Boram Yi¹, Tae Woo Oh², Seong-Ook Jung², Sanghun Jeon³, and Ji-Woon Yang¹ <i>¹Department of Electronic and Information Engineering, Korea University, ²School of Electrical and Electronic Engineering, Yonsei University, ³School of Electrical Engineering, KAIST</i></p>
<p>WD1-G-3 09:45-10:00</p>	<p>Novel Trap Profiling in Nitride Layer Using Space Program for 3-D NAND Flash Memory</p> <p>Jounghun Park, GilSang Yoon, Jaeseok Jin, DongHyun Go, and Jeong-Soo Lee <i>Department of Electrical Engineering, POSTECH</i></p>
<p>WD1-G-4 10:00-10:15</p>	<p>A Finite Element Simulation of a Full Switching Cycle in Resistive Memory</p> <p>Dongmyung Jung and Yongwoo Kwon <i>Department of Materials Science and Engineering, Hongik University</i></p>
<p>WD1-G-5 10:15-10:30</p>	<p>Investigation of Trap Profiles of Tunneling and Blocking Layers after P/E Cycling Stress in 3-D VNAND Flash Memory</p> <p>Gilsang Yoon, DongHyun Go, Jaeseok Jin, Jounghun Park, and Jeong-Soo Lee <i>Department of Electrical Engineering, POSTECH</i></p>