G. Device & Process Modeling, Simulation and Reliability 분과

2020년 2월 13일(목), 10:45-12:30 / Room D (사파이어 II+III, 5층)

[TD2-G] Atomistic Modeling

좌장: 이재우 교수 (고려대학교), 우지용 선임연구원 (한국전자통신연구원)

TD2-G-1 **10:45-11:15**	**[초청]** **Atomistic Molecular Dynamics Simulation for Semiconductor Processes Using Neural Network Potentials** Dongheon Lee, Kyeongpung Lee, Wonseok Jeong, Kyuhyun Lee, Dongsun Yoo, and Seungwu Han *Department of Materials Science and Engineering, Seoul National University*
TD2-G-2 **11:15-11:30**	**Investigation into the Effects of Ag Insertion Layer in TiN/SiN_x/TiN ReRAM through Monte Carlo Simulation** Yeon-Joon Choi[1], Min-Hwi Kim[1], Suhyun Bang[1], Tae-Hyeon Kim[1], Dong Keun Lee[1], Chae Soo Kim[1], Kyungho Hong[1], Seongjae Cho[2], and Byung-Gook Park[1] *[1]Inter-University Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Gachon University*
TD2-G-3 **11:30-11:45**	**Atomistic Study on Electronic Structures of Perovskite Heterojunctions: Enhancing Optical Properties with Light-induced Phase Separation** Hoon Ryu *KISTI*
TD2-G-4 **11:45-12:00**	**Modeling of the Conductive Oxygen Vacancies in the HfO_2 Supercell based on the First Principles Calculation** Junsung Park and Sung-min Hong *School of Electrical Engineering and Computer Science, GIST*
TD2-G-5 **12:00-12:15**	**Intrinsic Limit of Contact Resistance in $PtSe_2$ Mono-Multilayer Heterostructure** Eun Yeong Yang, Jae Eun Seo, Dongwook Seo, and Jiwon Chang *UNIST*
TD2-G-6 **12:15-12:30**	**Tunneling Electroresistance Effect Enhanced by Polar Interface in Hafniabased Ferroelectric Tunnel Junction** Junbeom Seo and Mincheol Shin *School of Electrical Engineering, KAIST*