G. Device & Process Modeling, Simulation and Reliability 분과

2020년 2월 14일(금), 15:45-17:15 / Room D (사파이어 II+III, 5층)

[FD3-G] Compact Modeling

좌장: 홍성민 교수 (GIST), 나현철 상무 (DB하이텍)

FD3-G-1 **15:45-16:00**	**Physics-based PcRAM Compact Model and Its Application to the SPICE Transient Simulation Considering the Ratio of Vertical/Lateral Crystal Growth Rate** Donguk Kim[1], Jun Tae Jang[1], Woo Sik Choi[1], Seojong Baek[1], Dong Myong Kim[1], Sung-jin Choi[1], Sanghyun Ban[2], Minchul Shin[2], Hanwool Lee[2], Hyungdong Lee[2], Hyun-sun Mo[1], and Dae hwan Kim[1] *[1]School of Electrical Engineering, Kookmin University, [2]SK Hynix Inc.*
FD3-G-2 **16:00-16:15**	**Compact Charge Model for Cylindrical Gate-All-Around MOSFETs Considering the Density-Gradient Equation** Kwang-woon Lee and Sung-min Hong *School of Electrical Engineering and Computer Science, GIST*
FD3-G-3 **16:15-16:30**	**New Large-signal Modeling for RF Kink Effect in Body Contacted PD-SOI nMOSFETs** Kiahn Lee and Seonghearn Lee *Department of Electronics Engineering, Hankuk University of Foreign Studies*
FD3-G-4 **16:30-16:45**	**Stretched Exponential Function-based SPICE Simulation Considering the Bias Stress Instability of IGZO TFTs** Youngjin Seo, Jun Tae Jang, Shinyoung Park, Jae-hyuck Kim, Dongyeon Kang, Sungju Choi, Jingyu Park, Dong Myong Kim, Sung-jin Choi, and Dae Hwan Kim *School of Electrical Engineering, Kookmin University*
FD3-G-5 **16:45-17:00**	**Accurate Modeling Methodology of LDMOS Leakage Current for ESD Protection Circuit Design** Jun Hyeok Kim *TE Modeling Team, DB HiTek*
FD3-G-6 **17:00-17:15**	**Negative Capacitance를 적용한 Gate-All-Around 트랜지스터의 동작 영역별 전류 모델** 배다현, 선윤근, 전종욱 *Department of Electrical and Electronic Engineering, Konkuk University*