

G. Device & Process Modeling, Simulation and Reliability 분과

2020년 2월 14일(금), 10:45-12:30 / Room D (사파이어 II+III, 5층)

■ [FD2-G] TCAD Simulation and Beyond

좌장: 최성진 교수 (국민대학교), 김성호 교수 (세종대학교)

FD2-G-1 10:45-11:00	Power, Performance and Area Analysis of Source/Drain Patterning n/p FinFETs Based 6T-SRAM Cell for 3-nm Technology Node Jun-Jong Lee, Jun-Sik Yoon, Seunghwan Lee, Jinsu Jeong, and Rock-Hyun Baek <i>Department of Electrical Engineering, POSTECH</i>
FD2-G-2 11:00-11:15	Prediction of the Electrostatic Potential Profile of a Semiconductor Device at Non-equilibrium by Using Deep Neural Networks Seung-cheol Han and Sung-min Hong <i>School of EECS, GIST</i>
FD2-G-3 11:15-11:30	High-voltage DeFinFET with a High-k Dielectric Field Plate Hyangwoo Kim, Hyeonsu Cho, and Chang-Ki Baek <i>Department of Creative IT Engineering, POSTECH</i>
FD2-G-4 11:30-11:45	채널 물질에 따른 Gate-all-around (GAA) Field Effect Transistor (FET) 의 Random Telegraph Noise (RTN) 특성 분석 Geunsoo Yang ¹ , Dong Hyun Kim ¹ , Dong Geun Park ¹ , Jungchun Kim ¹ , Sae Yan Choi ¹ , Sylvain Barraud ² , Laurent Bervard ² , and Jae Woo Lee ¹ <i>¹ICT Convergence Technology for Health & Safety and Department of Electronics and Information Engineering, Korea University, ²University of Grenoble Alpes, CEA-LETI</i>
FD2-G-5 11:45-12:00	Effects of the Gate Offset on Performance of Double-Gate Negative Capacitance Field-Effect Transistors Hyeongu Lee, Junbeom Seo, and Mincheol Shin <i>Department of Electrical Engineering, KAIST</i>
FD2-G-6 12:00-12:15	Study of Gallium Based Devices Using Multi-Subband Boltzmann Transport Equation Solver Suhyeong Cha and Sung-min Hong <i>School of Electrical Engineering and Computer Science, GIST</i>
FD2-G-7 12:15-12:30	Spacer Engineering of Double Gate MOSFET: Performance Study based on Quantum Transport Simulations Jihun Byun, Hyeongu Lee, and Mincheol Shin <i>School of Electrical Engineering, KAIST</i>