2020년 2월 13일(목), 09:00~10:30

Room H (하트 I, 6층)

N. VLSI CAD 분과
[TH1-N] System & Circuit Design Analysis and Optimization

TH1-N-1 **09:00~09:15**	**Loading-Effect-Aware Interface Model for SystemVerilog-SPICE Co-Simulation** Yanmei Li and Jaeha Kim *Department of Electrical and Computer Engineering, Seoul National University*
TH1-N-2 **09:15~09:30**	**Supply Voltage Analysis for Power Delay Optimization of Logic Design** Minju Kim, Daejeong Kim, and Hyunsun Mo *Department of Electronics Engineering, Kookmin University*
TH1-N-3 **09:30~09:45**	**Spike Counts Based Early Termination Scheme for Low Latency Neuromorphic Hardware** Geonho Kim, Taehwan Kimm, Seunghwan Bang, Hoyoung Tang, and Jongsun Park *Department of Electronic Engineering, Korea University*
TH1-N-4 **09:45~10:00**	**Spatial Correlation-aware Compression Algorithm for Energy-efficient CNN Accelerators** Yoonho Park, Yesung Kang, Sunghoon Kim, Eunji Kwon, and Seokhyeong Kang *Department of Electrical Engineering and Future IT Innovation Lab, POSTECH*
TH1-N-5 **10:00~10:15**	**2.5D Interposer Bus Routing for Multi-Flip Chip Designs** Sung-Yun Lee, Daeyeon Kim, Minhyuk Kweon, and Seokhyeong Kang *Department of Electrical Engineering, POSTECH*
TH1-N-6 **10:15~10:30**	**Designs of Converting Circuit between Binary and Ternary Logic** Seunghan Baek[1], Sunmean Kim[2], and Seokhyeong Kang[1] *[1]Department of Electrical Engineering, POSTECH, [2]Department of Electrical Engineering, UNIST*