2020년 2월 13일(목), 09:00~10:30

Room B (에메랄드 II+III, 5층)

F. Silicon and Group-IV Devices and Integration Technology 분과
[TB1-F] Emerging Device Technology I

TB1-F-1 **09:00~09:30**	**[초청]** **Optimization of Spacer and Source/Channel Junction to Improve TFET Characteristics** Garam Kim[1] and Sangwan Kim[2] *[1]Myongji University, [2]Ajou University*
TB1-F-2 **09:30~09:45**	**Switching Characteristics Analysis of Tunnel Field-effect Transistor with Elevated Drain by Changing Drain Underlap Length** Changha Kim[1], Kitae Lee[1], Junil Lee[1], Ryoongbin Lee[1], Sihyun Kim[1], Hyun-min Kim[1], Sangwan Kim[2] and Byung-Gook Park[1] *[1]Inter-University Semiconductor Research Center (ISRC) and Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electrical and Computer Engineering, Ajou University*
TB1-F-3 **09:45~10:00**	**Digital Inverter with Positive Feedback Field Effect Transistor** Changhoon Lee and Changhwan Shin *Department of Electrical and Computer Engineering, Sungkyunkwan University*
TB1-F-4 **10:00~10:15**	**A Novel Gate-normal Hetero-gate-dielectric (GHG) Tunnel Field-effect Transistors (TFETs)** Jang Woo Lee and Woo Young Choi *Department of Electronic Engineering, Sogang University*
TB1-F-5 **10:15~10:30**	**Capacitorless Double-Gate PNPN TFET 1T DRAM with SiGe Channel** Jae Seung Woo and Woo Young Choi *Department of Electronic Engineering, Sogang University*