

2020년 2월 14일(금), 15:45~17:15

Room D (사파이어 II+III, 5층)

G. Device & Process Modeling, Simulation and Reliability 분과

[FD3-G] Compact Modeling

FD3-G-1 15:45~16:00	Physics-based PcRAM Compact Model and Its Application to the SPICE Transient Simulation Considering the Ratio of Vertical/Lateral Crystal Growth Rate Donguk Kim ¹ , Jun Tae Jang ¹ , Woo Sik Choi ¹ , Seojong Baek ¹ , Dong Myong Kim ¹ , Sung-jin Choi ¹ , Sanghyun Ban ² , Minchul Shin ² , Hanwool Lee ² , Hyungdong Lee ² , Hyun-sun Mo ¹ , and Dae hwan Kim ¹ <i>¹School of Electrical Engineering, Kookmin University, ²SK Hynix</i>
FD3-G-2 16:00~16:15	Compact Charge Model for Cylindrical Gate-All-Around MOSFETs Considering the Density-Gradient Equation Kwang-woon Lee and Sung-min Hong <i>School of Electrical Engineering and Computer Science, GIST</i>
FD3-G-3 16:15~16:30	New Large-signal Modeling for RF Kink Effect in Body Contacted PD-SOI nMOSFETs Kiahn Lee and Seonghearn Lee <i>Department of Electronics Engineering, Hankuk University of Foreign Studies</i>
FD3-G-4 16:30~16:45	Stretched Exponential Function-based SPICE Simulation Considering the Bias Stress Instability of IGZO TFTs Youngjin Seo, Jun Tae Jang, Shinyoung Park, Jae-hyuck Kim, Dongyeon Kang, Sungju Choi, Jingyu Park, Dong Myong Kim, Sung-jin Choi, and Dae Hwan Kim <i>School of Electrical Engineering, Kookmin University</i>
FD3-G-5 16:45~17:00	Accurate Modeling Methodology of LDMOS Leakage Current for ESD Protection Circuit Design Jun Hyeok Kim <i>TE Modeling Team, DB HiTek</i>
FD3-G-6 17:00~17:15	Negative Capacitance를 적용한 Gate-All-Around 트랜지스터의 동작 영역별 전류 모델 배다현, 선윤근, 전종욱 <i>Department of Electrical and Electronic Engineering, Konkuk University</i>