G. Device & Process Modeling, Simulation and Reliability 분과
[FD1-G] Characterization of Semiconductor Devices

FD1-G-1 **09:00~09:15**	**Tunnel Oxide 내 Nitrogen Profile 에 따른 NAND Cell 동작 메커니즘 분석** 이현슬, 양형준, 권은미, 이봉훈, 이석규, 김진국 *Research and Development Division, SK Hynix*
FD1-G-2 **09:15~09:30**	**Modeling and Characterization of the Photovoltaic and Photoconductive Effects in Field Effect Transistors under Optical Illumination** Han Bin Yoo, Yoon Ju Park, Jintae Yu, Haesung Kim, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim *School of Electrical Engineering, Kookmin University*
FD1-G-3 **09:30~09:45**	**반도체 Integration 제작에서의 기계적 Stress 문제 해석 및 대응** 김민수, 서지웅, 김성동, 이석규, 김진국 *Research and Development Division, SK Hynix Inc.*
FD1-G-4 **09:45~10:00**	**Relationship between the Gate Bias and Stretched-exponential Function Model on the Positive Bias Stress-induced Charge Trapping in IGZO TFTs** Jae-hyuck Kim, Sungju Choi, YoungJin Seo, Jingyu Park, Ga Won Yang, In Seok Chae, Dong Myong Kim, Sung-jin Choi, and Dae Hwan Kim *School of Electrical Engineering, Kookmin Univresity*
FD1-G-5 **10:00~10:15**	**Extraction Method of Flat-band Voltage by Using Multi Frequency Capacitance-Voltage of a-IGZO Thin Film Transistors** In-seok Chae, Sungju Choi, YoungJin Seo, Jingyu Park, Jungi Min, Jae-hyuck Kim, Dong Myong Kim, Sung-jin Choi, and Dae Hwan Kim *School of Electrical Engineering, Kookmin University*
FD1-G-6 **10:15~10:30**	**VNAND Cell 온도 의존성 원인 분석을 위한 Polycrystalline Silicon Channel Trap 성분 추출법** 장호균[1], 임준영[1], 이현슬[1], 노일표[1], Nguyen MC[2], 최리노[2], 권은미[1], 이석규[1], 김진국[1] *[1]Research and Development Division, SK Hynix, [2]Department of Materials Science and Engineering, Inha University*