N. VLSI CAD 분과

2019년 2월 14일(목), 09:00-10:45
Room K (국실, 5층)

[TK1-N] Advances in Design Methodology

좌장: 정재용 교수(인천대학교), 양준성 교수(성균관대학교)

TK1-N-1 **09:00-09:15**	**FPGA Prototyping of Local Binary Convolutional Neural Network** Segi Lee, Aidyn Zhakatayev, and Jongeun Lee *School of Electrical & Computer Engineering, UNIST*
TK1-N-2 **09:15-09:30**	**Fault Influence on Deep Neural Network** 이서석, 양준성 *성균관대학교 반도체디스플레이공학과*
TK1-N-3 **09:30-09:45**	**FPGA Bitstream 분석 SW, BIL 연구** 김정현, 양준성 *성균관대학교 반도체디스플레이공학과*
TK1-N-4 **09:45-10:00**	**Performance Analysis Tool of FPGA Reverse Engineering** 조경국, 양준성 *성균관대학교 정보통신대학*
TK1-N-5 **10:00-10:15**	**Method of Detecting Voltage Drop at Power Distribution Networks with Simple Matrix Calculations** Jiyeon Lee and Jaeha Kim *Department of Electrical and Computer Engineering, Seoul National University*
TK1-N-6 **10:15-10:30**	**Estimating Performance Trade-off between Supply-Induced Jitter and Power Consumption of Clock Distribution Path for Memory I/O Block** Jiho Lee and Jaeha Kim *Department of Electrical and Computer Engineering, Seoul National University*
TK1-N-7 **10:30-10:45**	**Programmable Slope PTAT Temperature Sensor with Auto-Calibration** Ho-Jin Jeon, Dong-Gyu Kim, Sung-Jin Kim, and Kang-Yoon Lee *Department of Electrical and Computer Engineering, Sungkyunkwan University*