G. Device & Process Modeling, Simulation and Reliability 분과

2019년 2월 14일(목), 09:00-10:45
Room B (마루홀, 2층)

[TB1-G] Advanced Devices I : Multi-Gate Transistors

좌장: 홍성민 교수(GIST), 나현철 상무(DB하이텍)

TB1-G-1 **09:00-09:15**	**High Temperature Characterization of High-K/Metal-Gate 2-Stacked Gate-All-Around Nanowire FET Versus FinFET** Soo Hyun Kim[1], Dong Hyun Kim[1], Dong Geun Park[1], Doyoung Jang[2], and Jae Woo Lee[1] *[1]ICT Convergence Technology for Health & Safety and Department of Electronics and Information Engineering, [2]Imec, Belgium*
TB1-G-2 **09:15-09:30**	**Stress Analysis of Sub-7 nm P- and NMOS Gate-All-Around Transistor Processes on Si Bulk and SiGe-On-Insulator Substrates** Ji Hwan Lee, Kihwan Kim, and Saeroonter Oh *Department of Electrical Engineering, Hanyang University*
TB1-G-3 **09:30-09:45**	**Logic Performance of Multi-Stacked Gate-All-Around CMOS Transistors with Strain Incorporation** Kihwan Kim, Ji Hwan Lee, and Saeroonter Oh *Department of Electrical Engineering, Hanyang University*
TB1-G-4 **09:45-10:00**	**Threshold Voltage Variation Induced by Source/Drain Mole Fraction and Si/SiGe** Intermixing of Silicon Nanosheet Field-Effect Transistors Jinsu Jeong, Jun-Sik Yoon, Seunghwan Lee, and Rock-Hyun Baek *Department of Electrical Engineering, POSTECH*
TB1-G-5 **10:00-10:15**	**Layout Effect Analysis on Sub-10nm bulk-FinFET's Thermal Behaviors with Pre-existing EDA Software** Yoongeun Seon[1], Jaemin Han[1], Minsik Choi[1], Heesauk Jhon[2], and Jongwook Jeon[1] *[1]Department. of E.E Engineering, Konkuk University, [2]Department of E.I.C. Engineering, Mokpo National University*
TB1-G-6 **10:15-10:30**	**Physics Based Compact Model of Low-Frequency Noise for Gate-All-Around MOSFETs** Boram Yi[1], Geun Soo Yang[1], Sylvain Barraud[2], Laurent Bervard[1], Jae Woo Lee[1], and Ji-Woon Yang[1] *[1]Department of Electronic & Information Engineering, Korea University, [2]University of Grenoble Alpes, CEA-LETI, Minatec Campus, France*
TB1-G-7 **10:30-10:45**	**Low Frequency Noise Variability Analysis Depending on Epi-Source/Drain in GAA (Gate-All-Around) FET** Geun Soo Yang[1], Dong Hyun Kim[1], Dong Geun Park[1], Soo Hyun Kim[1], Jung Chun Kim[1], Sylvain Barraud[2], Laurent Bervard[2], and Jae Woo Lee[1] *[1]ICT Convergence Technology for Health & Safety and Department of Electronics and Information Engineering, [2]University of Grenoble Alpes, CEA-LETI, Minatec Campus, France*