B. Patterning 분과

2019년 2월 15일(금), 09:15-10:45
Room E (스카이홀, 2층)

[FE1-B] Advanced Patterning Process

좌장: 김현우 교수(한양대학교), 정지원 교수(인하대학교)

FE1-B-1 **09:15-09:30**	**플라즈마 표면 처리를 통한 산화갈륨 기반 FET의 문턱전압 제어 및 응용소자 제작** 김장혁, 김지현 *고려대학교 화공생명공학과*
FE1-B-2 **09:30-10:00**	**[초청]** **2D-MoS_2 Atomic Layer Etching** K. S. Kim[1], K. H. Kim[1], Y. J. Ji[1], and G. Y. Yeom[1,2] *[1]School of Advanced Materials Science and Engineering, Sungkyunkwan University,* *[2]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University*
FE1-B-3 **10:00-10:15**	**Dry Etching of SiO_2 Layers Using Fluoroether Compounds Having Low Global Warming Potential** Taehwan Cha[1], Yongjae Kim[2], Sangin Lee[1], Yegeun Cho[1], and Heeyeop Chae[1,2] *[1]School of Chemical Engineering, Sungkyunkwan University,* *[2]SKKU Advanced Institute of Nano Technology, Sungkyunkwan University*
FE1-B-4 **10:15-10:30**	**Resist-Free Fabrication of Three-Dimensional Silicon in a Single Chemical Process** Bugeun Ki[1,2], Keorock Choi[1,2], Kyunghwan Kim[1,2], and Jungwoo Oh[1,2] *[1]School of Integrated Technology, Yonsei University,* *[2]Yonsei Institute of Convergence Technology*
FE1-B-5 **10:30-10:45**	**Process Developing of Nanonet Structure Using Polystyrene Nanoparticles for High-Performance LTPS TFT Application** Gil Sang Yoon[1], Donghoon Kim[1], Iksoo Park[1], Bo Jin[1], and Jeong-soo Lee[1,2] *[1]Department of Electrical Engineering, POSTECH,* *[2]Division of IT-Convergence Engineering, POSTECH*