



## G. Device &amp; Process Modeling, Simulation and Reliability 분과

2019년 2월 15일(금), 15:30-17:15

Room B (마루홀, 2층)

**[FB3-G] Modeling & Simulation II : Memory and Other Devices**

좌장: 김성동 교수(SK하이닉스), 나현철 상무(DB하이텍)

<b>FB3-G-1</b> <b>15:30-15:45</b>	<b>A Comparative TCAD Study of Two Different Resistivity Models for Metal Word-Line of Highly-Scaled DRAM Cell Transistor</b> Dongyeon Oh, Jeenu Kim, Sangyong Kim, Seungcheol Lee, Seongdong Kim, Seokkiu Lee, and Jinkook Kim <i>Division of Research and Development, SK Hynix</i>
<b>FB3-G-2</b> <b>15:45-16:00</b>	<b>Virtual Reality Visualization Tool for Semiconductor Devices</b> Sung-Min Hong <i>EECS, GIST</i>
<b>FB3-G-3</b> <b>16:00-16:15</b>	<b>Observation of the Peroxide Formation and a Negative <math>\Delta V_T</math> under Current-Driving Condition in IZO TFTs with Self-Aligned Top-Gate Structure</b> Shinyoung Park, Sungju Choi, Jihyun Rhee, Dong Myong Kim, Sung-Jin Choi, and Dae Hwan Kim <i>School of Electrical Engineering, Kookmin University</i>
<b>FB3-G-4</b> <b>16:15-16:30</b>	<b>Performance Comparison between Conventional and Junctionless Transistors as 1T-DRAM Cell with Poly-Silicon Body</b> Hyeonjeong Kim <sup>1</sup> , Wookyung Sun <sup>1</sup> , In Man Kang <sup>2</sup> , Seongjae Cho <sup>3</sup> , and Hyungsoon Shin <sup>1</sup> <sup>1</sup> Department of Electronic and Electrical Engineering, Ewha Womans University, <sup>2</sup> School of Electronics Engineering, Kyungpook National University, <sup>3</sup> Department of Electronic Engineering, Gachon University
<b>FB3-G-5</b> <b>16:30-16:45</b>	<b>Empirical Model of Relationship between the Operation Frequency and the Size of Crossbar Array in the IGZO ReRAM-Based Reconfigurable Logic</b> Jingyu Park, Jun Tae Jang, Donguk Kim, Jungi Min, Geumho Ahn, Sung-Jin Choi, Dong Myong Kim, Hyun-Sun Mo, and Dae Hwan Kim <i>School of Electrical Engineering, Kookmin University</i>
<b>FB3-G-6</b> <b>16:45-17:00</b>	<b>Non-Linear Behavioral Modeling of SOI MOSFET for RF Switch Applications</b> Hyunjun Lee, Sangjun Lee, Seongsoo Park, Sung Moo Kim, and Hyunchul Nah <i>TE Modeling Team, DB HiTek</i>
<b>FB3-G-7</b> <b>17:00-17:15</b>	<b>A Novel Characterization Method to Extract for Intrinsic Contact Resistance of DRAM Peri. MOSFET</b> Tae Hun Kim, Tae Wook Kang, Yong Hyun Seo, Jae Hong Kim, and Dong Yean Oh <i>SK Hynix</i>