G. Device & Process Modeling, Simulation and Reliability 분과

2019년 2월 15일(금), 09:00-10:45
Room B (마루홀, 2층)

[FB1-G] Advanced Devices II : Nano Devices

좌장: 최성진 교수(국민대학교), 김성호 교수(세종대학교)

FB1-G-1 **09:00-09:15**	**Observation of Mobility and Velocity Behaviors in Ultra Scaled L_g=15 nm Silicon Nanowire pMOSFETs with Different Channel Diameters** Seunghwan Lee, Jun-Sik Yoon, Jinsu Jeong, and Rock-Hyun Baek *Department of Electrical Engineering, POSTECH*
FB1-G-2 **09:15-09:30**	**Interplay Between Line Edge Roughness and Interface Traps in Nanoplate VFETs** Yeaji Yoo[1,2], Kyul Ko[1,2], Myounggon Kang[3], Jongwook Jeon[4], and Hyungcheol Shin[1,2] *[1]Inter-University Semiconductor Research Center, Seoul Natioanl University,* *[2]School of Electrical Engineering and Computer Science, Seoul National University,* *[3]Department of Electronics Engineering, Korea National University of Transportation,* *[4]Department*
FB1-G-3 **09:30-09:45**	**The Parametric Study of Armchair Graphene Nanoribbon FET by NEGF Method** Ji-Hyun Hur *Department of Electrical Engineering, Sejong University*
FB1-G-4 **09:45-10:00**	**Si-Based Promising Two Dimensional Device : Si/GaP nFET** Bokyeom Kim and Mincheol Shin *School of Electrical Engineering, KAIST*
FB1-G-5 **10:00-10:15**	**Optimization of Vertical Nanowire Transistors for 3.5 nm Technology Node** Jaeyeol Park[1,2], Changbeom Woo[1,2], Shinkeun Kim[1,2], Dongjun Lee[1,2], Myounggon Kang[3], Jongwook Jeon[4], and Hyungcheol Shin[1,2] *[1]Inter-University Semiconductor Research Center, Seoul National University,* *[2]School of Electrical Engineering and Computer Science, Seoul National University,* *[3]Department of Electronics Engineering, Korea National University of Transportation,* *[4]Department of Electronics Engineering, Konkuk University*
FB1-G-6 **10:15-10:30**	**GaSb/InAs Heterojunction-Based UTB Tunnel FETs: A First-principles Study** Yucheol Cho, Yunhee Chang, and Mincheol Shin *School of Electronic Engineering, KAIST*
FB1-G-7 **10:30-10:45**	**Effect of Low Temperature on the Electron Mobility Enhancement of Strained-Si Nanowire Transistors** Geon-Tae Jang and Sung-Min Hong *School of Electrical Engineering and Computer Science, GIST*