2018년 2월 7일(수), 10:45-12:15
Room G (봉래II+III, 6층)

G. Device & Process Modeling, Simulation and Reliability 분과
[WG2-G] Advanced Devices III - Simulation and Reliability

좌장: 김성동 연구위원(SK 하이닉스), 최성진 교수(국민대학교)

WG2-G-1 **10:45-11:00**	**Threshold Voltage Shift of L-Shaped Tunnel Field-Effect Transistor for Better Performance** Faraz Najam and Yun Seop Yu *Department of Electrical, Electrical and Control Engineering and IITC, Hankyong National University*
WG2-G-2 **11:00-11:15**	**A Simulation Study on Tunneling Electroresistance Effect in Ferroelectric Tunnel Junction** Junbeom Seo, Moonhoi Kim, and Mincheol Shin *School of Electrical Engineering, KAIST*
WG2-G-3 **11:15-11:30**	**Investigation of Electrothermal Annealing to Repair the Hot-Carrier Degradation in a Tri-Gate FinFET** Joon-Kyu Han, Jun-Young Park, and Yang-Kyu Choi *School of Electrical Engineering, KAIST*
WG2-G-4 **11:30-11:45**	**Parasitic Capacitance Reduction on Tunneling Field Effect Transistor for Enhanced AC Performance and Energy Consumption** Jeesoo Chang, Sihyun Kim, Dae Woong Kwon, and Byung-Gook Park *Department of Electrical and Computer Engineering (ECE), Seoul National University*
WG2-G-5 **11:45-12:00**	**Analysis and Characterization of Dynamic Leakage Current in FinFETs and Its Compact Model for Gate-All-Around (GAA) MOSFETs** Boram Yi, Young-Hun Park, and Ji-Woon Yang *Department of Electronic & Information Engineering, Korea University*
WG2-G-6 **12:00-12:15**	**Strain Effectiveness of Gate-All-Around Si Transistors with Various Surface Orientations and Cross-Sections** Kihwan Kim and Saeroonter Oh *Division of Electrical Engineering, Hanyang University*